HIGH-FREQUENCY Y-PARAMETERS OF THE MOS TRANSISTOR

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ABSTRACT OF THE THESIS

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In this study the MOS transistor is treated as a transmission line with three coupled lines rather than as the more conventional two-line device. Two of the three lines represent the resistive channel and the gate which is capacitively coupled to the channel The addition of the third line, representing distributed capacitive coupling between the channel and the drain, accounts for Y_{12}, the reverse transfer admittance. Very good agreement is found between theoretical G_{12}, the real part of Y_{12}, and measured G_{12}. It is shown that $G_{12}>0$, indicating positive feedback within the device.

The unilateral power gain is formulated from the y-parameters and and shown to be, for a silicon-on-sapphire device,

$$U \approx \frac{45}{8} \mu_B \left(\frac{v_{sat}}{L}\right)^3 E_{ds} \frac{1}{T_s} \frac{\epsilon_{ox}}{\epsilon_s} \frac{1}{\omega^4}$$

where μ_B is the mobility in the bulk semiconductor, v_{sat} the saturation velocity of the carriers, E_{ds} the dielectric strength of the oxide, L the channel length, T_s the thickness of the semiconductor film, ϵ_{ox} the dielectric permittivity of the oxide, and ϵ_s the dielectric permittivity of the semiconductor. It is pointed out that since

present silicon devices operate close to the limits v_{sat} and E_{ds}, the device can be improved only by decreasing the film thickness or decreasing the channel length. More important is the advantage to be gained by using semiconductors with higher saturation velocities. It is shown that the unilateral power gain is inversely proportional to the semiconductor volume, thus a silicon-on-sapphire device is expected to be more useful at high frequencies than a bulk silicon device.

As a result of the internal positive feedback, the unilateral power gain would become infinite if the drain diode were entirely eliminated from the device. It is pointed out, however, that the diode is an inherent part of the device. It is shown that decreasing the silicon film thickness of silicon-on-sapphire devices will decrease the effects of the diode, thus improving the gain.

A circuit model is derived which has the proper y-parameters for all frequencies where the device has a gain greater than 1.

PREFACE

Acknowledgements

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Dedication

This thesis is dedicated to my wife, Martha Hopkins, whose tremendous cooperation in excess of five years has been appreciated more than can be described.

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CHAPTER I

Introduction

The purpose of this work is to describe the y-paramters of the MOS transistor under normal operating conditions at high frequencies. A model is proposed in Chapter III to account for the reverse transadmittance Y_{12}, which has not been adequately described in the literature. This model is formed by introducing distributed capacitance from drain to channel in the model proposed by J. R. Burns.[1]

An equation for the unilateral power gain is formulated from the new y-parameters in Chapter V. Basic physical limitations incorporated in this equation help to predict the best performance that one should expect from the MOS. It is shown that the drain-to-substrate diode has an extremely detrimental effect on the unilateral power gain.

A circuit model that yields the proper y-parameters at all but the highest useful frequencies is derived in Chapter VI.

Chapter VII gives data that shows the model is a good representation of actual device behavior.

Since the field-effect transistor (FET) is a relatively new device, a brief history and an outline of how the device is made are included here to introduce the device. Actually, the FET dates back to the 1920's.[2] J. E. Lilienfeld filed a U. S. patent disclosure "Device for Controlling Electric Current" in 1926[3] and two more in 1928.[4,5] The

materials he worked with included a copper-sulphur compound as the thin-film semiconductor material and glass as the substrate.

In 1935[6] Oskar Heil obtained a British patent entitled "Improvements in or Relating to Electrical Amplifiers and Other Control Arrangements and Devices". This patent described the use of a control electrode very close to a semiconductor layer of tellurium, iodine, cuprous oxide, or vanadium pentoxide. The function of the control electrode was to modulate current flow through the thin layer of semiconductor.

W. Shockley and G. L. Pearson in 1948[7] proposed a structure of germanium with a thin insulating sheet and evaporated metal on the thin insulating sheet. They theorized that by changing the voltage between the metal and the germanium, the conductivity of the germanium could be changed. By experiment they found that 90% of the charge induced in the germanium resided in traps at the germanium-insulator interface. The other 10% was induced mobile charge and did contribute to conductivity.

In 1952[8] Shockley devised the junction gate field-effect transistor, a device that avoided the surface effects. The field was created inside the semiconductor; thus, the surface had little to do with operation. Shockley called this device "unipolar" since only majority carrier flow occured. He also used "field effect" because conduction through the device was determined by a transverse field set up by the control electrode.

P. K. Weimer in the early 1960's[9] developed the thin-film transistor (TFT). He used cadmium sulfide as the semiconductor which was deposited on glass under vacuum.

S. R. Hofstein and F. P. Heiman applied Weimer's insulated gate concept to silicon technology. In 1963[10] they reported a new type of FET built with a metal-oxide-semiconductor (MOS) structure. The oxide physically separated the metal control electrode and the silicon.

The major difference between the MOS and Shockley's junction gate FET is in application of control voltages. The junction gate device may only have control voltages that back-bias the junction. The MOS may have both positive and negative control voltages.

The device of Hofstein and Heiman can be properly referred to as an MOS, FET, or insulated gate FET (IGFET). In this paper it is called MOS.

To fabricate the MOS, one begins with a piece of bulk silicon, either p or n type. P-type is described here. It is necessary to reverse p and n in the following example to fabricate the other device. All voltages would also be inverted. Two highly conducting n-type electrodes are diffused into the bulk. These electrodes are called the source and the drain. The source is grounded and the drain is held at a positive potential. The bottom surface of the bulk silicon is also grounded and is referred to as the substrate. The region between source and drain is called the channel. At this time there will

be no drain current since one essentially has a back-biased diode between the n-type drain contact and the p-type substrate. An oxide layer is grown over the channel and a metal plate is evaporated to cover the entire oxide layer. This metal plate is the control electrode and is referred to as the gate. This structure is shown in FIG. 1-1. If a positive potential is applied to the gate, holes will be driven down into the substrate from the channel and a layer of electrons (inversion layer) will form just below the oxide. These electrons will participate in current flow between the source and drain. Changing gate voltage changes the density of electrons, and thus changes the current.

The MOS, as shown in the following chapter, is a square law device. The drain current is a linear function of the square of the gate to source voltage. As a result, the MOS has excellent cross modulation distortion characteristics. It can be used quite easily as a detector. Biasing is simpler than with a bipolar transistor because the insulated input draws no dc current. The MOS lends itself to large-scale integration because it has an extremely simple structure. Since the MOS can be operated with either positive or negative gate voltages, and since it is possible to bias an MOS in such a way that it acts like a resistor, integrated circuits of MOS structures can be fabricated with no resistors and no capacitors.

The MOS has a major disadvantage in integrated circuits because all the devices have a common substrate. It has been shown that the substrate has a gating action[11] similar to the gate electrode. Thus, there is feedback to every other device from any one device. The substrate will also affect high-frequency response of the MOS. The MOS has been fabricated in another structure shown in FIG. 1-2. A thin film of silicon is grown on a sapphire substrate. The device is fabricated on this film the same way it is fabricated on bulk silicon. In this structure, every device in an integrated circuit is totally independent of all other devices. Because of the lack of the conducting substrate, the drain channel electrostatic coupling will have changed, thus the output conductance will also have changed.

CHAPTER II

Basic Theory of the MOS

The information in this chapter introduces the basic properties of the MOS. A similar treatment may be found in Field Effect Transistors by Wallmark and Johnson.[11]

For this discussion it is assumed that the semiconductor is p-type and uniformly doped. Furthermore, the contacts are n-type and the gate insulator thickness is much greater than the inversion layer thickness. The thickness of the inversion layer is a few Debye lengths. Typically, the Debye length is 10Å to 100Å, and the insulator thickness is 1000Å; hence the channel, or inversion layer, is merely a sheet charge. The entire voltage drop between gate and channel appears across the insulator. As a result, the channel conductivity is a simple calculation. By use of the "gradual channel approximation", which assumes that the rate of change of the drift field is much less than the rate of change of the gate field, the one-dimensional Poisson's Equation and Gauss' Law may be used to solve for the mobile charge in the channel.

The potential at some point x in the channel (see FIG 2-1) is given by V (x). It is obvious that

$$o \leq V(x) \leq V_D \qquad (2\text{-}1)$$

where V_D is the voltage from drain to ground. Grounded source operation is assumed. If $V_G > V_D$, the electric field terminating on charges in the channel is

$$E_z(x) = \frac{V_G - V(x)}{T_{ox}} - E_{ss} \tag{2-2}$$

where V_G is the voltage from gate to ground, T_{ox} is the insulator thickness, and E_{ss} is a built-in field resulting from charges permanently trapped at the semiconductor-insulator interface (surface states). Applying Gauss' Law

$$\sigma(x) = -\varepsilon_{ox} E_z(x) \tag{2-3}$$

where $\sigma(x)$ is the charge in the channel per unit area.

The familiar equation for the resistance of a block of material is

$$R = \rho \frac{L}{A} = \rho \frac{L}{WT} \tag{2-4}$$

The resistivity, ρ, is given by

$$\rho = \frac{1}{n e \mu} \tag{2-5}$$

where n is the carrier concentration, e the electronic charge, and μ the mobility. Combining (2-4) and (2-5) and inverting to obtain conductance,

$$G = n e \mu \frac{W T}{L} \tag{2-6}$$

The quantity neT of equation (2-6) is equivalent to a sheet charge. Thus, the conductance G(x) of an infinitesimal channel section of width W, length Δx, and mobility μ is given by

$$G(x) = - \sigma (x) \frac{\mu W}{\Delta x} \tag{2-7}$$

Ohm's Law gives the current passing through the infinitesimal element as

$$i = G(x) \Delta V(x) \tag{2-8}$$

This same current must pass through every element since there is no shunt. Then

$$I_D = \varepsilon_{ox} \mu W \left\{ \frac{V_G - V(x)}{T_{ox}} - E_{ss} \right\} \frac{\Delta V(x)}{\Delta x} \tag{2-9}$$

It is more convenient to represent E_{ss} as a voltage. Thus, define

$$V_T = E_{ss} T_{ox} \tag{2-10}$$

and call V_T the threshold voltage. V_T is the gate voltage at which conduction just begins and may be positive or negative. Then

$$I_D = \frac{\varepsilon_{ox} \mu W}{T_{ox}} \left\{ V_G - V_T - V(x) \right\} \frac{\Delta V(x)}{\Delta V} \tag{2-11}$$

Throughout the remainder of this paper it is assumed that $V_T = 0$. To account for the threshold voltage, it is necessary to replace V_G with $V_G - V_T$ everywhere V_G appears.

Integrating (2-11) from source to drain

$$\int_o^L I_D \, dx = \int_o^{V_D} \frac{\epsilon_{ox} \mu W}{T_{ox}} [V_G - V(x)] \, dV(x) \tag{2-12}$$

$$I_D = \frac{\epsilon_{ox} \mu W}{2T_{ox} L} [2V_D V_G - V_D^2] \tag{2-13}$$

As the drain voltage is increased, the electric field in the oxide near the drain is reduced. From (2-2),

$$E_z (L) = \frac{V_G - V_D}{T_{ox}} \tag{2-14}$$

In fact, when $V_D = V_G$, there is no field and thus no inversion layer at that point. Increasing V_D above V_G, the point in the channel at which $E_z(x) = 0$ moves toward the source. Label ℓ_s the distance from the source to the $E_z(x) = 0$ point. The remaining distance to the drain is labeled ℓ_d. Then

$$\ell_s + \ell_d = L \tag{2-15}$$

The region ℓ_d is depleted. All drifting charges upon reaching ℓ_s are injected into ℓ_d and move to the drain in this high field region. The potential at ℓ_s is V_G by definition of ℓ_s. From continuity of current,

$$\int_o^{\ell_s} I_D \, dx = \int_o^{V_G} \frac{\epsilon_{ox} \mu W}{T_{ox}} [V_G - V(x)] \, dV(x) \tag{2-16}$$

$$I_D = \frac{\epsilon_{ox}\,\mu W}{2T_{ox}\ell_s}\,V_G^2 \tag{2-17}$$

This equation for I_D has two variables, V_G and ℓ_s. Obviously, ℓ_s varies with some combination of V_D and V_G. It is extremely difficult to calculate ℓ_s because of the complex nature of the field in the drain region. Various attempts have been made to calculate ℓ_s. In general, however, it is found that

$$\ell_s \approx L \tag{2-18}$$

and, therefore

$$I_{DS} = \frac{\epsilon_{ox}\,\mu W}{2T_{ox}L}\,V_G^2 \tag{2-19}$$

where the S denotes saturation. The transconductance and output conductance in saturation become

$$g_{mo} = \frac{\partial I_D}{\partial V_G}\Big|_{V_D} = \frac{\epsilon_{ox}\,\mu W}{T_{ox}L}\,V_G \tag{2-20}$$

$$g_{DS} = \frac{\partial I_D}{\partial V_D}\Big|_{V_G} = 0 \tag{2-21}$$

This device is a square law device and the characteristic curves in saturation are flat. This is shown in FIG. 2-2, a plot of equations (2-13) and (2-19) with various constants assumed. FIG. 2-3 shows the I-V characteristics of an actual device.

The potential in the channel as a function of x will now be derived. Begin with (2-16), which assumes saturation, but drop the limits on the integrals.

$$\int I_D \, dx = \int \frac{\epsilon_{ox} \mu W}{T_{ox}} [V_G - V(x)] \, dV(x) \tag{2-22}$$

$$I_D x + \text{Const.} = \frac{\epsilon_{ox} \mu W}{T_{ox}} [V_G V(x) - 1/2 \, V^2(x)] \tag{2-23}$$

$$V^2(x) - 2 V_G V(x) = \frac{-2T_{ox}}{\mu W \epsilon_{ox}} I_{DS} x + \frac{-2T_{ox}}{\mu W \epsilon_{ox}} \text{Const.} \tag{2-24}$$

Completing the square,

$$V^2(x) - 2V_G V(x) + V_G^2 = V_G^2 - \frac{2T_{ox}}{\mu W \epsilon_{ox}} I_{DS} x - \frac{2T_{ox}}{\mu W \epsilon_{ox}} \text{Const.} \tag{2-25}$$

$$V(x) = V_G \left\{ 1 \pm \sqrt{1 - \frac{2T_{ox}}{\mu W \epsilon_{ox}} \frac{I_{DS} x}{V_G^2} - \frac{2T_{ox}}{\mu W \epsilon_{ox}} \frac{\text{Const.}}{V_G^2}} \right\} \tag{2-26}$$

Substituting the boundary condition $V(0) = 0$

$$0 = V_G \left\{ 1 \pm \sqrt{1 - 0 - \frac{2T_{ox}}{\mu W \epsilon_{ox}} \frac{\text{Const.}}{V_G^2}} \right\} \tag{2-27}$$

Thus, the sign is negative and

$$\frac{2T_{ox}}{\mu W \epsilon_{ox}} \frac{\text{Const.}}{V_G^2} = 0 \tag{2-28}$$

Now substituting from (2-19) for I_{DS}

$$V(x) = V_G \left\{ 1 - \sqrt{1 - \frac{x}{L}} \right\} \qquad (2\text{-}29)$$

CHAPTER III

DC Output Conductance and Capacitance

The assumptions made in this chapter are the same as in the previous chapter. Saturation is also assumed so that, from (2-19) and (2-20)

$$I_{DS} = \frac{\epsilon_{ox}\mu W}{2T_{ox}L} V_G^2 \tag{3-1}$$

$$g_{mo} = \frac{\epsilon_{ox}\mu W}{T_{ox}L} V_G \tag{3-2}$$

By definition C_{GC} is the total gate-to-channel capacitance and C_{DC} is the total drain-to-channel capacitance. Then

$$C_{GC} = \frac{\epsilon_{ox} W L}{T_{ox}} \tag{3-3}$$

The model of Hofstein and Heiman[10] is used to calculate C_{DC}. The field lines between the drain and the underside of the channel as shown in FIG. 3-1 are semicircles. Hofstein and Heiman say that this feedback effect must be calculated by an incremental technique, but as a first assumption the model presented should suffice. Then the incremental capacitance from the drain to a section of channel dx in length is simply

$$d(C_{DC}) = \frac{\epsilon_s W}{\pi(L-x)} dx \tag{3-4}$$

Then

$$C_{DC} = \int_0^{\ell_s} \frac{\epsilon_s W}{\pi(L-x)}\, dx \tag{3-5}$$

$$= \frac{\epsilon_s W}{\pi} \ell n \left| \frac{L}{L-\ell_s} \right| \tag{3-6}$$

Utilizing (2-15)

$$C_{DC} = \frac{\epsilon_S W}{\pi} \ell n \left| \frac{L}{\ell_d} \right| \tag{3-7}$$

Now ℓ_d is the length of the space-charge-limited region and depends upon V_D and perhaps V_G. In practice it is found that

$$\frac{L}{\ell_d} \sim 10 - 100 \tag{3-8}$$

This is a large range, but the log of this number reduces an error of 10 to an error of 2. Thus,

$$C_{DC} \approx \epsilon_s W \tag{3-9}$$

A change in the drain voltage of ΔV_D causes a change in the average channel charge per unit length of

$$\Delta Q = \frac{C_{DC}\Delta V_D}{L} \tag{3-10}$$

This change in charge secs an average channel field in the active region of

$$E_{av} = \frac{V_G}{L} \tag{3-11}$$

Thus, the change in drain current can be written as

$$\Delta I_{DS} = \Delta Q \; E_{av} \; \mu \tag{3-12}$$

or

$$g_{DS} = \frac{\Delta I_{DS}}{\Delta V_D} \Big|_{V_G} = \frac{C_{DC}}{L} \; \frac{V_G}{L} \; \mu \tag{3-13}$$

Substituting (3-9)

$$g_{DS} = \frac{\epsilon_s W \mu}{L^2} \; V_G \tag{3-14}$$

By combining equations (2-20), (3-3), (3-9), and (3-14),

$$g_{DS} = \frac{C_{DC}}{C_{GC}} \; g_{mo} \tag{3-15}$$

Defining D as the ratio of C_{DC} to C_{GC}

$$D = \frac{C_{DC}}{C_{GC}} \tag{3-16}$$

Finally

$$g_{DS} = D \; g_{mo} \tag{3-17}$$

Now g_{mo} and g_{DS} will be calculated using a new model given in FIG. 3-2. This model provides the capacitive coupling of the Hofstein

and Heiman model, but keeps the capacitance distributed. Following the method of Chapter II,

$$\sigma(x) = -\frac{C_{GC}}{L}\,(V_G - V(x)) - \frac{C_{DC}}{L}\,(V_D - V(x)) \tag{3-18}$$

$$= \frac{-1}{L}\,(C_{GC} + C_{DC})\left[\frac{C_{GC}V_G + C_{DC}V_D}{C_{GC} + C_{DC}} - V(x)\right] \tag{3-17}$$

Substituting D as defined in (3-16)

$$\sigma(x) = \frac{-1}{L}\,C_{GC}\,(1 + D)\left[\frac{V_G + D\,V_D}{1 + D} - V(x)\right] \tag{3-20}$$

Defining C_T and V_{ST} as

$$C_T = C_{GC}\,(1 + D) \tag{3-21}$$

$$V_{ST} = \frac{V_G + D\,V_D}{1 + D} \tag{3-22}$$

equation (3-20) becomes

$$\sigma(x) = -\frac{C_T}{L}\,(V_{ST} - V(x)) \tag{3-23}$$

V_{ST} will be referred to as the steering voltage.

The calculation for the saturation current can now be completed.

$$\int_o^{\ell_s} I_D\,dx = \mu\,\frac{C_T}{L}\int_o^{V_{ST}} (V_{ST} - V(x))\,dV(x) \tag{3-24}$$

The limit has become V_{ST} since $V(x) = V_{ST}$ is the point where the inversion layer terminates.

Completing the integration and assuming as before that $\ell_s \approx L$, the current is found to be

$$I_{DS} = \frac{\mu C_T}{2L^2} V_{ST}^2 \tag{3-25}$$

$$= \frac{\mu \epsilon_{ox} W}{2 L T_{ox}} (1 + D) V_{ST}^2 \tag{3-26}$$

Thus

$$g_{mo} = \frac{\partial I_D}{\partial V_G} \Big|_{V_D} = \frac{\mu C_T}{L^2} \left(\frac{V_G + D V_D}{1 + D}\right) \left(\frac{1}{1 + D}\right) \tag{3-27}$$

$$g_{DS} = \frac{\partial I_{DS}}{\partial V_D} \Big|_{V_G} = \frac{\mu C_T}{L^2} \left(\frac{V_G + D V_D}{1 + D}\right) \left(\frac{D}{1 + D}\right) \tag{3-28}$$

$$= D\, g_{mo} \tag{3-29}$$

Note that this model gives the same relationship between g_{DS} and g_{mo} as the model of Hofstein and Heiman. The value of D in terms of geometry can be obtained from (3-3), (3-9), and (3-16) and is given by

$$D = \frac{\epsilon_s T_{ox}}{\epsilon_{ox} L} \tag{3-30}$$

Expanding (3-26)

$$I_{DS} = \frac{\mu \epsilon_{ox} W}{2LT_{ox}} \frac{1}{1 + D} (V_G^2 + 2DV_G V_D + D^2 V_D^2) \tag{3-31}$$

The primary difference between (3-31) and (2-19) is that V_D appears in (3-31). The term linear in V_D gives rise to a tilt in the I-V characteristics which agrees with experiment. The term with V_D^2 becomes non-negligible when $V_D \sim 2V_G/D$. For typical devices this means $V_D \sim 30V_G$. However, if V_D is large, or D is increased, this model will give an output current dependent upon V_D^2. This also is in agreement with experiments by Richman.[12]

For future reference V(x) is needed. Following the procedure of Chapter II, it is found that

$$V(x) = V_{ST} \left\{1 - \sqrt{1 - \frac{x}{L}}\right\} \tag{3-32}$$

This model has one fault that should be discussed. The incremental capacitor, $\frac{C_{DC}}{L}$, has been assumed uniform over the entire length of the channel, Actually, the incremental capacitor should be given by a Taylor series as

$$\frac{C_{DC}}{L} = a_o + a_1 x + a_2 x^2 + a_3 x^3 + \ldots \tag{3-33}$$

Here it has been assumed that a_i, where $i \neq o$, is small compared to a_o. This is not strictly true, but it does serve as a first approximation.

CHAPTER IV

High-Frequency Behavior

The model proposed in the previous chapter may be used to calculate the y-parameters of the MOS as a function of frequency. The model is a transmission line consisting of three lines: one is resistive, the other two are capacitively coupled to the first. By writing mesh and node equations, two differential equations are obtained. Next, by utilizing the concept of a steering voltage, the differential equations are manipulated into a form that has been solved. This solution gives the steering current that must then be manipulated back into its original components to yield the y-parameters.

FIG. (4-1), used in writing the differential equations, is identical to FIG. (3-2) except that a different notation is used. Several different currents are specified and each is explained below. The drain current is composed of two parts, I_{d1} and I_{d2}. I_{d2} is that portion of the drain current which flows through the drain-to-channel capacitance. I_{d1} is the drain current which flows only through the channel. $I(x,t)$ is the current in the channel as a function of position and time. I_g is the gate current and I_s is the source current.

The current entering node i is given by

$$I(x,t) - I(x,t) - \Delta I\ (x,t) + \frac{C_{GC}\Delta x}{L} \frac{\partial}{\partial t} (V_G(t) - V(x,t)) + \frac{C_{DC}\Delta x}{L} \frac{\partial}{\partial t} (V_D(t) - V(x,t)) = 0 \qquad (4\text{-}1)$$

$$\frac{\Delta I(x,t)}{\Delta x} = \frac{C_{GC}}{L} \frac{\partial}{\partial t} (V_G(t) - V(x,t)) + \frac{C_{DC}}{L} \frac{\partial}{\partial t} (V_D(t) - V(x,t)) \tag{4-2}$$

In the limit $\Delta x \to o$

$$\frac{\partial I(x,t)}{\partial x} = \frac{C_{GC}}{L} \frac{\partial}{\partial t} (V_G(t) - V(x,t)) + \frac{C_{DC}}{L} \frac{\partial}{\partial t} (V_D(t) - V(x,t)) \tag{4-3}$$

$$= \frac{1}{L} (C_{GC} + C_{DC}) \frac{\partial}{\partial t} \left[\frac{C_{GC}V_G(t) + C_{DC}V_D(t)}{C_{GC} + C_{DC}} - V(x,t)\right] \tag{4-4}$$

$$= \frac{1}{L} C_{GC} (1 + D) \frac{\partial}{\partial t} [V_{ST}(t) - V(x,t)] \tag{4-5}$$

Summing the voltages around the mesh j gives

$$V_G(t) - V(x,t) + V(x,t) + \Delta V(x,t) - V_G(t) - \bar{R}\Delta x\, I(x,t) = 0 \tag{4-6}$$

$$\frac{\Delta V(x,t)}{\Delta x} = \bar{R}\, I(x,t) \tag{4-7}$$

In the limit $\Delta x \to o$

$$\frac{\partial V(x,t)}{\partial x} = \bar{R}\, I(x,t) \tag{4-8}$$

Note that the diagram in FIG. 4-2 satisfies (4-5) and (4-8). This three line problem has been transformed into the two line problem of Burns.[1] Define

$$\bar{G} = \bar{R}^{-1} \tag{4-9}$$

Then

$$I(x,t) = \bar{G} \frac{\partial V(x,t)}{\partial x} \tag{4-10}$$

Also

$$\bar{G} = -\mu \sigma (x,t) \tag{4-11}$$

Utilizing (3-18)

$$\bar{G} = \mu \left[\frac{C_{GC}}{L} (V_G(t) - V(x,t)) + \frac{C_{DC}}{L} (V_D(t) - V(x,t))\right] \tag{4-12}$$

$$= \frac{\mu}{L} C_{GC} (1 + D) [V_{ST}(t) - V(x,t)] \tag{4-13}$$

Taking the derivative of (4-10)

$$\frac{\partial I(x,t)}{\partial x} = \frac{\partial \bar{G}}{\partial x} \frac{\partial V(x,t)}{\partial x} + \bar{G} \frac{\partial^2 V(x,t)}{\partial x^2} \tag{4-14}$$

$$\frac{\mu C_{GC}(1 + D)}{L} \left[\frac{\partial}{\partial x} (V_{ST}(t) - V(x,t) \frac{\partial V(x,t)}{\partial x} + (V_{ST}(t)-V(x,t)) \frac{\partial^2 V(x,t)}{\partial x^2}\right] \tag{4-15}$$

Define

$$\bar{V}(x,t) = V_{ST}(t) - V(x,t) \tag{4-16}$$

$$\frac{\partial \bar{V}(x,t)}{\partial x} = - \frac{\partial V(x,t)}{\partial x} \tag{4-17}$$

Equation (4-5) becomes

$$\frac{\partial I(x,t)}{\partial x} = \frac{C_{GC}(1 + D)}{L} \frac{\partial}{\partial t} \bar{V}(x,t) \tag{4-18}$$

Equation (4-15) becomes

$$\frac{\partial I(x,t)}{\partial x} = \frac{\mu C_{GC}(1 + D)}{L} \left[\frac{\partial}{\partial x} \bar{V}(x,t) \frac{\partial}{\partial x} \bar{V}(x,t) + \bar{V}(x,t) \frac{\partial^2}{\partial x^2} \bar{V}(x,t)\right] \tag{4-19}$$

Equating (4-18) and (4-19)

$$\frac{1}{\mu} \frac{\partial}{\partial t} \bar{V}(x,t) = \left(\frac{\partial}{\partial x} \bar{V}(x,t)\right)^2 + \bar{V}(x,t) \frac{\partial^2}{\partial x^2} \bar{V}(x,t) \tag{4-20}$$

This equation must be solved for $\bar{V}(x,t)$. The form of equation (4-20) is identical to the equation solved by Burns.[1] The solution of (4-20) is given in full in the Appendix. Only the results are given here.

$$i_{d1}(s) = g_{mo}(1 + D) v_{ST}(s) \frac{1}{1 + \frac{4}{15}\frac{s}{\omega_o} + \frac{1}{45}\left(\frac{s}{\omega_o}\right)^2 + \frac{4}{4455}\left(\frac{s}{\omega_o}\right)^3 + \ldots} \tag{4-21}$$

$$i_{ST}(s) = g_{mo}(1 + D) v_{ST}(s) \frac{\frac{2}{3}\frac{s}{\omega_o} + \frac{4}{45}\left(\frac{s}{\omega_o}\right)^2 + \frac{2}{405}\left(\frac{s}{\omega_o}\right)^3 + \ldots}{1 + \frac{4}{15}\frac{s}{\omega_o} + \frac{1}{45}\left(\frac{s}{\omega_o}\right)^2 + \frac{4}{4455}\left(\frac{s}{\omega_o}\right)^3 + \ldots} \tag{4-22}$$

$$\omega_o = \frac{\mu V_{ST}}{L^2} \tag{4-23}$$

$$v_{ST}(t) = V_{ST}(t) - V_{ST} \tag{4-24}$$

It is necessary to separate $i_{ST}(s)$ into its two components $i_g(s)$ and $i_{d2}(s)$. From FIG. 4-1

$$i_{d2}(x,s) = s \frac{C_{DC}}{L} \Delta x \, (V_D(s) - V(x,s)) \tag{4-25}$$

$$i_{d2}(s) = \int_o^L s \frac{C_{DC}}{L} (V_D(s) - V(x,s)) \, dx \tag{4-26}$$

$$= s \, C_{DC} V_D(s) - s \frac{C_{DC}}{L} \int_o^L V(x,s) \, dx \tag{4-27}$$

$$i_g(x,s) = s \frac{C_{GC}}{L} \Delta x \, (V_G(s) - V(x,s)) \tag{4-28}$$

$$i_g(s) = \int_o^L \frac{sC_{GC}}{L} (V_G(s) - V(x,s)) \, dx \tag{4-29}$$

$$= sC_{GC} V_G(s) - s \frac{C_{GC}}{L} \int_o^L V(x,s) \, dx \tag{4-30}$$

Rewriting (4-27) and (4-30)

$$\frac{1}{L} \int_o^L V(x,s) \, dx = V_D(s) - \frac{1}{sC_{DC}} i_{d2}(s) \tag{4-31}$$

$$\frac{1}{L} \int_o^L V(x,s) \, dx = V_G(s) - \frac{1}{sC_{GC}} i_g(s) \tag{4-32}$$

Then from (4-31) and (4-32)

$$\frac{C_{DC}}{C_{GC}} i_g(s) - i_{d2}(s) = sC_{DC}(V_G(s) - V_D(s)) \tag{4-33}$$

or

$$D\, i_g(s) - i_{d2}(s) = s\, D\, C_{GC}\, (V_G(s) - V_D(s)) \tag{4-34}$$

From comparison of FIGS. 4-1 and 4-2, it can be seen that

$$i_g(s) + i_{d2}(s) = i_{ST}(s) \tag{4-35}$$

Simultaneous solution of (4-34) and (4-35) yields

$$i_g(s) = \frac{i_{ST}(s) + s\, D\, C_{GC}(V_G(s) - V_D(s))}{1 + D} \tag{4-36}$$

$$i_{d2}(s) = \frac{D\, i_{ST}(s) + s\, D\, C_{GC}(V_D(s) - V_G(s))}{1 + D} \tag{4-37}$$

The y-parameters are derived from (4-21), (4-36), and (4-37), but first, a parasitic aspect of all MOS structures must be considered.

The drain-substrate interaction in the device shown in FIG. 1-1 behaves like a reverse-biased diode. As a result, the drain sees a series resistor-capacitor to gound.[13] The capacitance is equal to the diode capacitance. The resistor comes from the resistivity of the substrate which is electrically connected to the source. Thus, y_{22} is increased by the term

$$y_{22} = y'_{22} + \frac{s\,C_{ds}}{1 + s\,R_s C_{ds}} \tag{4-38}$$

The silicon-on-sapphire device of FIG. 1-2 does not have the silicon substrate so it would seem that the parasitic RC is not present. However, this is not the case. With a bias applied to gate and drain, there is a region at the source end of the silicon that is not depleted since the potential of the channel close to the source is nearly zero. Thus, the same situation exists as above. There is depletion capacitance from the drain to the non-depleted source region and resistance associated with this source region. As a result, (4-38) applies in all cases. The R and C may be different but they are present.

For convenience define

$$A_d(s) = \frac{1}{1 + \frac{4}{15}\frac{s}{\omega_o} + \frac{1}{45}\left(\frac{s}{\omega_o}\right)^2 + \frac{4}{4455}\left(\frac{s}{\omega_o}\right)^3 + \ldots} \tag{4-39}$$

$$A_g(s) = \frac{\frac{2}{3}\frac{s}{\omega_o} + \frac{4}{45}\left(\frac{s}{\omega_o}\right)^2 + \frac{2}{405}\left(\frac{s}{\omega_o}\right)^3 + \ldots}{1 + \frac{4}{15}\frac{s}{\omega_o} + \frac{1}{45}\left(\frac{s}{\omega_o}\right)^2 + \frac{1}{4455}\left(\frac{s}{\omega_o}\right)^3 + \ldots} \tag{4-40}$$

Then (4-21), (4-36), and (4-37) become

$$i_{d1}(s) = g_{mo}\,A_d(s)\,\left\{V_g(s) + D\,V_d(s)\right\} \tag{4-41}$$

$$i_{d2}(s) = D\,g_{mo}\,A_g(s)\left\{V_g(s) + D\,V_d(s)\right\} + s\,\frac{D\,C_{GC}}{1 + D}\left\{V_d(s) - V_g(s)\right\} \tag{4-42}$$

$$i_g(s) = g_{mo} A_g(s) \left\{ V_g(s) + D\ V_d(s) \right\} + s \frac{D\ C_{GC}}{1 + D} \left\{ V_g(s) - V_D(s) \right\} \qquad (4\text{-}43)$$

Taking the parasitic RC into account

$$i_{d3}(s) = \frac{s\ C_{ds}}{1 + s\ R_s C_{ds}}\ V_d(s) \qquad (4\text{-}44)$$

Finally

$$i_d(s) = i_{d1}(s) + i_{d2}(s) + i_{d3}(s) \qquad (4\text{-}45)$$

From the definition of the y-parameters

$$y_{11} = \frac{\partial I_g(s)}{\partial V_g(s)} \Big|_{V_d(s)} \qquad (4\text{-}46a)$$

$$y_{12} = \frac{\partial I_g(s)}{\partial V_d(s)} \Big|_{V_g(s)} \qquad (4\text{-}46b)$$

$$y_{21} = \frac{\partial I_d(s)}{\partial V_g(s)} \Big|_{V_d(s)} \qquad (4\text{-}46c)$$

$$y_{22} = \frac{\partial I_d(s)}{\partial V_d(s)} \Big|_{V_g(s)} \qquad (4\text{-}46d)$$

Equations (4-41) - (4-44) yield for the y-parameters of the MOS

$$y_{11} = g_{mo}\ A_g(s) + s \frac{D\ C_{GC}}{1 + D} \qquad (4\text{-}47a)$$

$$y_{12} = D\ g_{mo}\ A_g(s) - s \frac{D\ C_{GC}}{1 + D} \qquad (4\text{-}47b)$$

$$y_{21} = g_{mo} A_d(s) + D\, g_{mo} A_g(s) - s \frac{D\, C_{GC}}{1 + D} \qquad (4\text{-}47c)$$

$$Y_{22} = D\, g_{mo} A_d(s) + D^2 g_{mo} A_g(s) + \frac{s\, C_{DS}}{1 + s\, C_{ds} R_s} + s \frac{D}{1+D} C_{GC} \qquad (4\text{-}47d)$$

Experimental results relevant to equations (4-47) are considered in Chapter VII. It is shown that these equations are a good representation of actual device behavior.

CHAPTER V

Unilateral Power Gain

Mason has described the unilateral power gain,[14] the maximum neutralized power gain, as

$$U = \frac{|y_{21} - y_{12}|^2}{4(G_{11}G_{22} - G_{12}G_{22})} \tag{5-1}$$

Utilizing equations (4-47)

$$U = \frac{|A_d(s)|^2}{4D\left[\mathrm{Re}\left\{A_g(s)\right\}\mathrm{Re}\left\{A_d(s) + DA_g(s) + \frac{sC_{ds}}{Dg_{mo}(1+sC_{ds}R_s)}\right\} - \mathrm{Re}\left\{A_d(s)+DA_g(s)\right\}\overline{\mathrm{Re}\left\{A_g(s)\right\}}\right]} \tag{5-2}$$

$$= \frac{g_{mo}\,|A_d(s)|^2}{4\ \mathrm{Re}\left\{A_g(s)\right\}\ \mathrm{Re}\left\{\frac{s\,C_{ds}}{1 + s\,C_{ds}R_s}\right\}} \tag{5-3}$$

$$= \frac{g_{mo}}{4}\,\frac{1 + \omega^2 C_{ds}{}^2 R_s{}^2}{\omega^2 C_{ds}{}^2 R_s}\,\frac{|A_d(s)|^2}{\mathrm{Re}\left\{A_g(s)\right\}} \tag{5-4}$$

$$|A_d(s)|^2 = A_d(s)\,A_d^*(s) \tag{5-5}$$

where $A_d^*(s)$ is the complex conjugate of $A_d(s)$

Define $A_g(s) = P(s)/D(s)$ (5-6)

$$A_d(s) = 1/D(s) \tag{5-7}$$

$$\text{Then } |A_d(s)|^2 = \frac{1}{D(s)} \cdot \frac{1}{D(-s)} \tag{5-8}$$

$$\text{Re}\left\{A_g(s)\right\} = \text{Re}\left\{\frac{P(s)}{D(s)}\,\frac{D(-s)}{D(-s)}\right\} \tag{5-9}$$

$$= \frac{\text{Re}\left\{P(s) \cdot D(-s)\right\}}{D(s)\cdot D(-s)} \tag{5-10}$$

Then

$$U = \frac{g_{mo}}{4}\,\frac{1 + \omega^2 C_{ds}{}^2 R_s{}^2}{\omega^2 C_{ds}{}^2 R_s}\,\frac{1}{\text{Re}\left\{P(s) \cdot D(-s)\right\}} \tag{5-11}$$

$$P(s) \cdot D(-s) = \left[\frac{2}{3}\frac{s}{\omega_o} + \frac{4}{45}\left(\frac{s}{\omega_o}\right)^2 + \frac{2}{405}\left(\frac{s}{\omega_o}\right)^3 + \frac{2}{13365}\left(\frac{s}{\omega_o}\right)^4 + \ldots\right]$$

$$\left[1 - \frac{4}{15}\frac{s}{\omega_o} + \frac{1}{45}\left(\frac{s}{\omega_o}\right)^2 - \frac{4}{4455}\left(\frac{s}{\omega_o}\right)^3 + \ldots\right] \tag{5-12}$$

$$\text{Re}\left\{P(s) \cdot D(-s)\right\} = -\frac{8}{45}\left(\frac{s}{\omega_o}\right)^2 + \frac{4}{45}\left(\frac{s}{\omega_o}\right)^2 - \frac{8}{13365}\left(\frac{s}{\omega_o}\right)^4 + \frac{4}{2025}\left(\frac{s}{\omega_o}\right)^4$$

$$- \frac{8}{6075}\left(\frac{s}{\omega_o}\right)^4 + \frac{2}{13365}\left(\frac{s}{\omega_o}\right)^4 + \ldots \tag{5-13}$$

$$= \frac{-4}{45}\left(\frac{s}{\omega_o}\right)^2 + .00021\left(\frac{s}{\omega_o}\right)^4 + \ldots \tag{5-14}$$

The second term is truly negligible.

Thus

$$\text{Re}\left\{P(j\omega)\cdot D(-j\omega)\right\} = \frac{4}{45}\left(\frac{\omega}{\omega_o}\right)^2 \tag{5-15}$$

$$U = \frac{45}{16}\, g_{mo}\, \frac{1+\omega^2 C_{ds}^2 R_s^2}{\omega^2 C_{ds}^2 R_s}\left[\frac{\omega_o}{\omega}\right]^2 \tag{5-16}$$

Define

$$\omega_s = \frac{1}{C_{ds} R_s} \tag{5-17}$$

Then

$$U = \frac{45}{16}\, g_{mo}\, \frac{1+\left(\frac{\omega}{\omega_s}\right)^2}{C_{ds}^2 R_s}\, \frac{\omega_o^2}{\omega^4} \tag{5-18}$$

In general, $\omega_s \gg \omega_o$ so that (5-18) becomes

$$U = \frac{45}{16}\, g_{mo}\, \frac{1}{C_{ds}^2 R_s}\, \frac{\omega_o^2}{\omega^4} \tag{5-19}$$

This theory has been based upon the existence of a drain to channel capacitance of value DC_{GC}. Note, however, that equation (5-19) is essentially independent of D. Both g_{mo} and ω_o have a small second order dependence upon D. This factor D does play an extremely important role, though, in the derivation of equation (5-19). This can be seen by an examination of the denominator of equation (5-1).

$$DEN = 4\,(G_{11}\, G_{22} - G_{12}\, G_{21}) \tag{5-20}$$

It should be obvious from equations (4-47) that

$$G_{12} = D\, G_{11} \tag{5-21}$$

$$G_{22} = D\, G_{21} + G_{ds} \tag{5-22}$$

where

$$G_{ds} = \frac{\omega^2 C_{ds}^2 R_s}{1 + \omega^2 C_{ds}^2 R_s^2} \tag{5-23}$$

Then

$$DEN = 4\ (D\ G_{11}\ G_{21} + G_{11}\ G_{ds} - D\ G_{11}\ G_{21}) \tag{5-24}$$

$$= 4\ G_{11}\ G_{ds}$$

The cancellation that occurs in (5-24) occurs only because of D. What is happening is that the MOS has positive feedback from drain to channel. Note that $G_{12}>0$ indicating positive feedback.

Consider briefly the possibility that either $C_{ds}=0$ or $R_s=0$. Then $G_{ds}=0$ and as a result DEN=0. The positive feedback causes the unilateral gain to become infinite if there is no resistive load. This result clearly indicates the extremely detrimental effect of the parasitic drain diode on the unilateral power gain. As stated in the previous chapter, this diode is present even in silicon-on-sapphire devices. Thus, rather than discuss what would happen if the diode were not there, it would be more constructive to attempt to learn more about the diode.

Consider a piece of semiconductor of thickness T, width W, and length L. Very highly conducting semiconductor of opposite type is

placed on one end. The depletion capacitance when back-biased with V volts is

$$C = WT\sqrt{\frac{\epsilon eN}{2V}} \tag{5-26}$$

where ϵ is the dielectric permittivity of the semiconductor, N is the carrier concentration, and e is the electronic charge. The resistance of this structure, assuming depletion depth is much smaller than the structure length, is

$$R = \frac{L}{WT}\ \frac{1}{\mu_B eN} \tag{5-27}$$

where μ_B is the mobility in the bulk semiconductor. Then

$$C^2R = WTL\ \frac{\epsilon}{2\mu_B V} \tag{5-28}$$

In the case of a bulk silicon device, the highly conducting contact is the drain and the other contact is the bottom of the substrate. Since the drain is a much smaller contact, an extremely complicated fringe field exists making it virtually impossible to apply equation (5-28) in a meaningful way.

Equation (5-28) indicates that C^2R is proportional to the volume of the semiconductor. Since a silicon-on-sapphire device has significantly less volume of semiconductor than a bulk silicon device for the same transistor parameters, it would appear that C^2R is smaller for

the silicon-on-sapphire device. If T_s is defined as the thickness of the silicon film, equation (5-28) becomes

$$C^2_R = W\ T_s L\ \frac{\epsilon_s}{2\mu_B V_D} \tag{5-29}$$

This equation is not strictly true because of depletion by the gate and, as was mentioned earlier, the decrease of resistor length due to depletion by the drain. Only the non-depleted semiconductor contributes to the resistance.

Keeping these deficiencies in mind, equation (5-19) may be rewritten for a silicon-on-sapphire device as

$$U = \frac{45}{16}\ g_{mo}\ \frac{2\ \mu_B V_D}{W\ T_s L\ \epsilon_s}\ \frac{\omega_o^2}{\omega^4} \tag{5-30}$$

Substituting for ω_o and g_{mo}

$$U = \frac{45}{8}\ \frac{\mu_B\ \mu^3\ V_{ST}^3\ V_D}{L^6 T_{ox} T_s}\ \frac{\epsilon_{ox}}{\epsilon_s}\ \frac{1}{\omega^4} \tag{5-31}$$

Here μ_B has been kept separate from μ since they refer to different mobilities, μ being the mobility in the channel while μ_B is the mobility of the semiconductor bulk.

Equation (5-31) gives the unilateral power gain as a function of basic parameters. Thus the equation immediately specifies what must be done to increase the unilateral power gain: increase μ, V_{ST}, V_D, or ϵ_{ox}; decrease L, T_{ox}, T_s or ϵ_s. Increasing the voltages increases

fields which are already approaching critical values. To increase a voltage, a dimension must also be increased, thus producing no net change in U. As a result, equation (5-31) is not much help in understanding gain limitations. Physical limitations must be specified in the equation for U.

One of the limitations is the carrier saturation velocity. For low fields $v = \mu E$. For very large fields $v = v_{sat}$. Thus there is a limitation

$$\left(\frac{\mu V_{ST}}{L}\right)_{max} = v_{sat} \tag{5-32}$$

The value of v_{sat} for electrons in silicon is approximately 10^5 meters per second. Another limitation is the dielectric strength of the oxide. Thus

$$\left(\frac{V_G}{T_{ox}}\right)_{max} = E_{ds} \tag{5-33}$$

E_{ds} is about $6 \cdot 10^8$ volts per meter for SiO_2. Assume that $V_g \approx V_D$. Equation (5-31) becomes

$$U \approx \frac{45}{8} \mu_B \left(\frac{v_{sat}}{L}\right)^3 E_{ds} \frac{1}{T_s} \frac{\epsilon_{ox}}{\epsilon_s} \frac{1}{\omega^4} \tag{5-34}$$

The quantity v_{sat}/L is called the transit time. This factor enters (5-34) since it requires a finite time to move energy from the source end of the transistor to the drain end. Either a shorter channel

length or a material with higher saturation velocity will give larger U. The bulk mobility and semiconductor thickness enter (5-34) since these parameters represent loss in the bulk semiconductor due to the charging of the drain diode. E_{ds} enters representing the maximum gate to channel coupling. Increasing ϵ_{ox} will increase this coupling while increasing ϵ_s increases the effect of the drain diode.

An attempt has been made in this chapter to use the y-parameters to determine the high-frequency limitations of the MOS. The unilateral power gain was used as the "figure of merit". Equation (5-34) can be used to predict the highest frequency at which the MOS will operate with a power gain. Present devices operate close to the limits of v_{sat} and E_{ds}. Thus for a silicon device, since μ_B is a property of the material, the present limitations are the dimensions of L and T_s. Decreasing either will improve the device according to the formula

$$\omega_T \propto \left(\frac{1}{L}\right)^{3/4} \left(\frac{1}{T_s}\right)^{1/4} \tag{5-35}$$

It should be noted that decreasing L will force the device to operate in a mode different from that assumed in deriving the transistor parameters. Thus it may be found that decreasing L decreases the unilateral power gain since the entire device behavior may be altered. It appears that decreasing T_s is truly a good way to improve the

the device. The limitation at present is the lack of technology for actually making a thinner film of semiconductor. It is obvious that the ultimate limit would be in terms of atomic layers.

CHAPTER VI

Circuit Model for the MOS

A circuit model for the MOS which is good to frequencies as high as $4\ \omega_o$, a frequency where most present devices have a power gain less than 1, is derived here. Consider only those terms in equations (4-47) of order s. The coefficient of the s term in the denominator is changed from 4/15 to 1/6 to help make up for the loss of all the other terms. In some of the equations, the effect of the s^2 term in the numerator is as large as the effect of terms of lower order, thus some correction is needed. This is a compromise between terms using A_g and those using A_d. Then the real and imaginary parts of the y-parameters may be written as

$$G_{11} = \frac{\frac{1}{9}\, g_{mo} \left(\frac{\omega}{\omega_o}\right)^2}{1 + \left(\frac{\omega}{6\omega_o}\right)^2} \tag{6-1a}$$

$$B_{11} = \frac{\frac{2}{3}\, g_{mo} \frac{\omega}{\omega_o}}{1 + \left(\frac{\omega}{6\omega_o}\right)^2} + \omega \frac{D}{1 + D} C_{GC} \tag{6-1b}$$

$$G_{12} = \frac{\frac{1}{9}\, D\, g_{mo} \left(\frac{\omega}{\omega_o}\right)^2}{1 + \left(\frac{\omega}{6\omega_o}\right)^2} \tag{6-1c}$$

$$B_{12} = \frac{\frac{2}{3}\, D\, g_{mo} \frac{\omega}{\omega_o}}{1 + \left(\frac{\omega}{6\omega_o}\right)^2} - \omega \frac{D}{1 + D} C_{GC} \tag{6-1d}$$

$$G_{21} = \frac{g_{mo}\left\{1 + \frac{1}{9} D \left(\frac{\omega}{\omega_o}\right)^2\right\}}{1 + \left(\frac{\omega}{6\omega_o}\right)^2} \tag{6-1e}$$

$$B_{21} = -\frac{\frac{1}{6} g_{mo}\left\{1 - 4 D\right\}\frac{\omega}{\omega_o}}{1 + \left(\frac{\omega}{6\omega_o}\right)^2} - \omega \frac{D}{1 + D} C_{GC} \tag{6-1f}$$

$$G_{22} = \frac{D\, g_{mo}\left\{1 + \frac{1}{9} D \left(\frac{\omega}{\omega_o}\right)^2\right\}}{1 + \left(\frac{\omega}{6\omega_o}\right)^2} + \frac{\omega^2 C_{ds}^2 R_s}{1 + \omega^2 C_{ds}^2 R_s^2} \tag{6-1g}$$

$$B_{22} = \frac{\omega C_{ds}}{1 + \omega^2 C_{ds}^2 R_s} - \frac{\frac{1}{6} D\, g_{mo}\left\{1 - 4D\right\}\frac{\omega}{\omega_o}}{1 + \left(\frac{\omega}{6\omega_o}\right)^2} + \omega \frac{D}{1 + D} C_{GC} \tag{6-1h}$$

These equations are given so that they may be compared with the exact equations for the y-parameters. The circuit model derived below will have precisely these y-parameters. FIG. 6-1 compares these equations with the exact equations of Chapter IV.

In deriving the circuit model, recognize first from equations (4-47) that the term $s \frac{D}{1+D} C_{GC}$ which appears in all four y-parameters is a capacitance from drain to gate. A capacitance from input to output will appear as $+sC$ in Y_{11} and Y_{22} and will appear as $-sC$ in Y_{12} and Y_{21}. Recognize also the $R_s C_{ds}$ term as being a series RC from drain to source.

By defining A_g' as A_g with terms higher than s deleted (and 4/15 changed 1/6) and A_d' as A_d changed in the same way, it can be

recognized readily that A_g' represents a series RC while A_d' represents the voltage across the C in the same series RC. Thus Y_{11} is represented by a series RC where C=2/3 C_{GC} and R=1/(4g_{mo}) and $g_{mo}A_d'$ in Y_{21} represents a current generator from drain to source of value $g_{mo}v_1$ where v_1 is the voltage on the Y_{11} capacitor. Also D^2A_g' in Y_{22} is a series RC where C=2/3 D^2C_{GC} and R=1/(4D^2g_{mo}) while the term DA_d' in Y_{22} can be represented as another current source from drain to source of value $Dg_{mo}v_2$ where v_2 is the voltage across the Y_{22} capacitor.

There are two terms in the y-parameters not yet realized for this model. These terms are DA_g' in Y_{12} and Y_{21}. By recognizing that A_g' is really the current through a series RC, Y_{12} can be realized as a current generator from gate to source of values i_2/D where i_2 is the current through the Y_{22} series RC. Likewise, DA_g' in Y_{21} can be realized as a current generator from drain to source of value Di_1 where i_1 is the current through the Y_{11} series RC.

This circuit is shown in FIG. 6-2. Note that the Y_{12} current generator i_2/D is really amplifying the current that flows through the Y_{22} capacitor since 1/D>1. The polarity of this generator produces the positive feedback mentioned in Chapter VI. The $Dg_{mo}v_2$ generator produces the dc output conductance of the MOS since at low frequencies $v_2=v_d$ and thus, $i_d=Dg_{mo}v_d$. The Di_1 current generator attenuates the current that flows through the Y_{11} capacitor since D<1. This current

will be significantly smaller than the other parts of the drain current for normal devices, thus this generator could be deleted in using the model. Likewise, the current i_2 is so small that the Y_{22} RC could be deleted except that i_2 is the current that is amplified to produce Y_{12}.

Dawson[13] has proposed a circuit model for the MOS based on empirical evidence. This model is shown in FIG. 6-3. Setting $C_1 = 2/3\ C_{GC}$, $C_2 = DC_1$, and $g_{do} = Dg_{mo}$, gives the parameters

$$G_{11} = \frac{\frac{1}{9} g_{mo} \left(\frac{\omega}{\omega_o}\right)^2}{1 + \left(\frac{1+D}{6} \frac{\omega}{\omega_o}\right)^2} \tag{6-2a}$$

$$B_{11} = \frac{\frac{2}{3} g_{mo} \frac{\omega}{\omega_o} + \frac{1}{54} D\ (1+D)\ g_{mo} \left(\frac{\omega}{\omega_o}\right)^3}{1 + \left(\frac{1+D}{6} \frac{\omega}{\omega_o}\right)^2} \tag{6-2b}$$

$$G_{12} = \frac{\frac{1}{9} D\ g_{mo} \left(\frac{\omega}{\omega_o}\right)^2}{1 + \left(\frac{1+D}{6} \frac{\omega}{\omega_o}\right)^2} \tag{6-2c}$$

$$B_{12} = - \frac{\frac{1}{54} D\ (1+D)\ g_{mo} \left(\frac{\omega}{\omega_o}\right)^3}{1 + \left(\frac{1+D}{6} \frac{\omega}{\omega_o}\right)^2} \tag{6-2d}$$

$$G_{21} = \frac{g_{mo} \left\{1 + \frac{1}{9} D \left(\frac{\omega}{\omega_o}\right)^2\right\}}{1 + \left(\frac{1+D}{6} \frac{\omega}{\omega_o}\right)^2} \tag{6-2e}$$

$$B_{21} = - \frac{\frac{1}{6} g_{mo}(1+D) \frac{\omega}{\omega_o} + \frac{1}{54} g_{mo} D(1+D) \left(\frac{\omega}{\omega_o}\right)^3}{1 + \left(\frac{1+D}{6} \frac{\omega}{\omega_o}\right)^2} \qquad (6\text{-}2f)$$

$$G_{22} = \frac{D\, g_{mo} \left\{1 + \frac{1}{9} D \left(\frac{\omega}{\omega_o}\right)^2\right\}}{1 + \left(\frac{1+D}{6} \frac{\omega}{\omega_o}\right)^2} + \frac{\omega^2 C_{ds}{}^2 R_s}{1 + \omega^2 C_{ds}{}^2 R_s{}^2} \qquad (6\text{-}2g)$$

$$B_{22} = \frac{\omega\, C_{ds}}{1 + \omega^2 C_{ds}{}^2 R_s{}^2} + \frac{\frac{1}{2} D\, g_{mo}(1-\frac{D}{3})\frac{\omega}{\omega_o} + \frac{1}{54} D(1+D) g_{mo} \left(\frac{\omega}{\omega_o}\right)^3}{1 + \left(\frac{1+D}{6} \frac{\omega}{\omega_o}\right)^2} \qquad (6\text{-}2h)$$

By assuming typical values of D (D<.1) and assuming ωC_{ds} dominates in B_{22}, all parts of (6-2) and (6-1) are essentially identical with the single exception of B_{12}. Equation (6-1d) gives $B_{12} \alpha\omega$ while equation (6-2d) gibes $B_{12} \alpha\omega^3$. The experimental evidence given in the following chapter indicates $B_{12} \alpha\omega$. This, of course, could be the result of parasitic capacitance, but the data from some devices is extremely close to that predicted by (6-1d). By adding a capacitor of value $1/3\ DC_{GC}$ from drain to gate in the model of FIG. 6-3, for typical values of D, this model will give essentially the same results as the model of FIG. 6-2.

CHAPTER VII

Measurements

The theory proposed in this thesis accounts for Y_{12}. Both Y_{11} and Y_{21} have been well described by Burns.[1] Dawson[13] has described quite well the effect of the drain diode on Y_{22}. This theory yields results almost identical to those of Burns for Y_{11} and Y_{21}, and the drain diode was included here to obtain good results for Y_{22}. Thus, measurements of Y_{12} must be made and compared to values predicted here to confirm or deny the theory.

The theory states that G_{12} is given by

$$G_{12} = D\, G_{11} \tag{7-1}$$

At frequencies up to ω_o this becomes

$$G_{12} = \frac{1}{9} D\, g_{mo} \left(\frac{\omega}{\omega_o}\right)^2 \tag{7-2}$$

From equation (3-17)

$$D = g_{DS}/g_{mo} \tag{7-3}$$

Equations (7-2) and (7-3) give

$$G_{12} = \frac{1}{9} g_{DS} \left(\frac{\omega}{\omega_o}\right)^2 \tag{7-4}$$

Low-frequency measurements of g_{DS}, g_{mo} and C_{GC} can be substituted in (7-4) to predict high-frequency performance of G_{12}. However, it

usually is found when measuring G_{12} that B_{12} is so much larger than G_{12} that accurate results cannot be obtained for G_{12}. Thus a device suitable for the measurement must be found.

The intrinsic part of B_{12} at frequencies up to 4 ω_o is approximately

$$B_{12} = -\frac{D}{3} g_{mo} \frac{\omega}{\omega_o} \tag{7-5}$$

The parasitic, or extrinsic, capacitance must be minimized. The extrinsic capacitance has two distinct components -- the first is that arising from inter-electrode capacitance in the device; the second is that due to the header, capacitance between the bonding posts, etc. Assume the first is proportional to the gate area, LW, and that the second is constant. Then

$$B_{12} = -\frac{D}{3} g_{mo} \frac{\omega}{\omega_o} - \omega K_1 LW - \omega K_2 \tag{7-6}$$

where K_1 and K_2 are constants. Form the quantity R as the ratio of $-B_{12}$ and G_{12}.

$$R = \frac{-B_{12}}{G_{12}} = 3 \frac{\omega_o}{\omega} + 9 \frac{K_1 LW}{DC_{GC}} \frac{\omega_o}{\omega} + 9 \frac{K_2}{DC_{GC}} \frac{\omega_o}{\omega} \tag{7-7}$$

It is desired to maximize G_{12} and minimize R. From (7-7) measurements must be made at very high frequencies to reduce ω_o/ω. This conveniently increases G_{12} since $G_{12} \alpha (\omega/\omega_o)^2$. Assume the measurements are made at ω_o so that $\omega/\omega_o = 1$. In that case

$$G_{12} = \frac{1}{9} D g_{mo} \tag{7-8}$$

$$R = 3 + 9 \frac{K_1 LW}{DC_{GC}} + 9 \frac{K_2}{DC_{GC}} \tag{7-9}$$

Substituting for D, G_{mo}, and C_{GC}

$$G_{12} = \frac{1}{9} \mu \epsilon_s \frac{W}{L^2} V_{ST} (1 + D) \tag{7-10}$$

$$R = 3 + 9 \frac{K_1 L}{\epsilon_s} + 9 \frac{K_2}{\epsilon_s W} \tag{7-11}$$

Equation (7-10) illustrates that as large a bias as possible should be used. The only other variables are W and L.

$$G_{12} = k_1 \frac{W}{L^2} \tag{7-12}$$

$$R = k_2 + k_3 L + k_4/W \tag{7-13}$$

where k_1, k_2, k_3, and k_4 are constants. From this information the table of FIG. 7-1 can be formed. From the table it is obvious that to optimize the measurement of G_{12}, L must be decreased and W increased. Since decreasing L increases ω_o, decrease L to the point that measurements can just be made at ω_o. A table similar to that of FIG. 7-1 assuming ω constant instead of ω/ω_o constant would show that decreasing L makes measurements more difficult. Thus it cannot be permitted that ω_o become so large that it is impossible to make measurements at ω_o.

Measurements were made on several transistors. Only three gave useable results for G_{12}. In all other cases, R was a large number because of parasitic capacitance. The measured Y_{12} is given in FIG. 7-2 through FIG. 7-4 for the 3N142, the 40468, and a triode fabricated by Dawson. For the theoretical curves, it is assumed that all extrinsic capacitances are zero. Thus the discrepancy between measured and theoretical B_{12} is due to the extrinsic capacitance. It is considered very significant that the measured and theoretical G_{12} are so similar. The parasitic capacitance does not affect G_{12}.

FIG. 7-5 gives measured and theoretical values for all four y-parameters for the 40468. FIG. 7-6 gives the theoretical unilateral power gain from equation (5-19) and compares it with that obtained from calculations using the measured values of FIG. 7-5 in equation (5-1).

The actual measurements were not y-parameters, but were scattering parameters. The conversion from s-parameters to y-parameters is given below.

$$Y_{11} = \frac{1}{50} \frac{(1-s_{11})(1+s_{22}) + s_{12}\, s_{21}}{DEN} \tag{7-14}$$

$$Y_{12} = -\frac{1}{25} \frac{s_{12}}{DEN} \tag{7-15}$$

$$Y_{21} = -\frac{1}{25} \frac{s_{21}}{DEN} \tag{7-16}$$

$$Y_{22} = \frac{1}{50} \frac{(1 + s_{11})(1 - s_{22}) + s_{12}\, s_{21}}{DEN} \tag{7-17}$$

where

$$DEN = (1 + s_{11})(1 + s_{22}) - s_{12}\, s_{21} \tag{7-18}$$

The factor 1/50 enters because of the 50 Ω system. The s-parameters are defined as

$s_{11(22)}$: Reflection coefficient of the input (output) with the output (input) terminated in 50Ω.

$s_{12(21)}$: Ratio of power transmitted through the device to the power incident at the input (output) of the device.

The components used in measuring s-parameters are a vector voltmeter, two dual directional couplers, two bias-tees, a jig for the device, two variable-length-lines, and five 50Ω terminations. The voltmeter is a sampling RF voltmeter with two inputs. Magnitudes of each input and their relative phase are measured. The sampling rate is 20 KHz and the frequency range is 1 MHz to 1000 MHz. The dual directional coupler is a device that separates incident and reflected power on a line. The dual directional couplers used have a VSWR of 1.1 and provide incident and reflected powers attenuated 20 db. The frequency range is 100 MHz to 2000 MHz. The bias-tees permit application of dc voltages to the device under test. The

VSWR is less than 1.2 and useful frequency range is 100 MHz to 3000 MHz. This set-up is illustrated in FIG. 7-7.

The first step in measuring s-parameters is calibration of the equipment. To measure s_{11} it is necessary that the distance from the generator to the probe measuring the incident power be identical to the distance from the generator to the device under test and back to the probe measuring the reflected power. To establish this relationship a short is placed at the point where the device is to be measured. A variable-length-line is placed between the dual directional coupler port that has an output proportional to the incident power and the probe that measures this power. The length of the line is adjusted so the phase difference of the reflected and incident voltage is 180^{o} since the reflection coefficient of a short is -1. The magnitude of the two voltages should be equal. If the two distances are equal, changing the frequency of the generator does not change the phase reading of 180^{o}. A rough setting is obtained at lower frequencies and the "fine tuning" is done at the highest frequency. The calibration for s_{22} is identical to the procedure described for s_{11} except all references are to the components on the output side of the device. The calibration for s_{21} consists of inserting a feed-through at the location of the test point and adjusting the length from the generator to the probe measuring incident power to be equal to the length from the generator through the point of test

to the probe measuring power coming out of the device. The proper setting is obtained when the phase meter reads 0^{o}.

If the test-point is midway between the dual directional couplers, the last adjustment is already correct. In this case, only one variable-length-line is necessary. The equipment used for the measurements were the HP 8405A Vector Voltmeter, the HP 8745A S-Parameter Test Set, the HP 608F 10-480 MHz signal generator, and the HP 612A 450-1230 MHz signal generator. The Test Set contains all components in FIG. 7-7. Rather than use two variable-length-lines, the instrument employs a switching arrangement that permits proper application of the generator, location of the variable-length-line, and location of the measuring probes. Once this single line is adjusted, no re-adjustments are necessary for any s-parameter.

The s-parameters are obtained from the measured voltages and phases according to the relationship

$$|s_{11}| = |(V_{ri}/V_{ii})_{V_2 = 0}| \qquad (7\text{-}19)$$

$\text{Arg}(s_{11})$ = Angle indicated on vector voltmeter when V_{ii} is on probe A and V_{ri} is on probe B.

Similar relationships apply for s_{12}, s_{21}, and s_{22}.

CHAPTER VIII

Conclusions

Burns suggested in his Ph. D. thesis[1] that the output admittance of the MOS be studied because of its increase at high frequencies. It is pretty well accepted in the field that this increase is a result of a diode from drain-to-substrate. It has been proposed here that this diode is present even in silicon-on-sapphire devices; Dawson[13] has shown that the output admittance of the silicon-on-sapphire device increases at high frequencies. As discussed in Chapter V, this diode seriously inhibits the unilateral power gain of the MOS. If the diode were absent the gain would become infinite. However, this diode appears to be an inherent part of the device. One way to decrease the effect of the diode is to fabricate the device on sapphire rather than on bulk silicon and make the silicon film as thin as possible.

Further work should be done to explain fully the effects of this diode. The only effect of the diode in the unilateral power gain is the term R^2C which is proportional to semiconductor volume to first order. However, the bulk silicon device should have a smaller R than the same size device fabricated on sapphire, even though it has greater semiconductor volume, because the area through which the diode current flows is greater. At the same time, C^2

increases because of the greater area. It would appear that C^2 increases faster than R decreases, thus the device on sapphire would appear to be better. However, this is far from conclusive evidence. Dawson[13] has shown that decreasing the area of the drain decreases C^2R. He has also shown that a silicon-on-sapphire device has a smaller C^2R than the same device on bulk silicon. No strong relationship has been shown, only trends. The extreme fringing field encountered in the bulk silicon device and the complicated depletion characteristics of the silicon-on-sapphire device certainly require more study. In view of the fact that this diode is so detrimental to unilateral power gain, it demands that the mechanism be fully understood.

The expression for G_{12} derived here is positive, indicating positive feedback. This fact was also confirmed experimentally. It is interesting to note that so little attention has been paid in the past to the fact that $G_{12}>0$. In 1966 Fischer[15] proposed a model for the MOS. He published data showing $G_{12}>0$ for two different transistors and said "...whenever y_{12r} was large enough to be detected at high frequencies, it was found to be positive. No simple lumped network could provide enough phase shift to make y_{12r} positive." The data sheet for the RCA 3N142 indicates that $G_{12}>0$ at very high frequencies. It appears that most experimenters, though, have not

been able to measure G_{12} because of the typically much larger B_{12} which swamps out G_{12}. Chapter VII describes the type of device necessary to be able to measure G_{12}.

One interesting result not yet discussed is the behavior of Y_{22} at higher frequencies. It was shown that if it were not for the drain diode

$$G_{22} = D\, G_{21} \tag{8-1}$$

Since G_{21} becomes negative at higher frequencies, it is expected that G_{22} would also go negative. It may never be possible to prove this, though, because it is not clear that the diode can be made small enough to see this effect.

It is also interesting to compare the model of Dawson given in Chapter VI with the model presented here. There is a very strong resemblance between Dawson's model and the incremental model of Chapter IV - the incremental model is very much like many of Dawson's models cascaded. Thus it is not surprising that so many of the y-parameters from the two models are similar. What really becomes interesting, though, is the fact that Dawson's model does not have a term in B_{12} proportional to ω, yet the model presented here does. The distributed model has two ω terms in B_{12}-- one is approximately $+2/3\ DC_{GC}$; the other is $-\ DC_{GC}$. The result is $-1/3\ DC_{GC}$. The conclusion seems to be that the distributed nature of the model presented

here keeps these two terms from being identical as seems to occur in the bulk model.

More work need also be done in trying new semiconductor materials for the MOS. Since the unilateral gain is approximately proportional to the cube of the saturation velocity and since the mobility of the non-depleted semiconductor enters the unilateral power gain equation, significant improvement could be made in this area.

The primary theme that has been presented here is that there is capacitive feedback from the drain to the channel and that this feedback can yield extremely high power gain if the drain diode effect is reduced. The idea of capacitance feedback was first presented by Heiman and Hofstein, but only for dc calculations. Johnson[16] proposed an empirical model utilizing this capacitance to account for a positive G_{12}. Dawson refined Johnson's model somewhat by incorporating the dc drain conductance in this feedback. The goal here has been to propose a physical model with a distributed capacitance and show that the capacitance does truly give rise to a positive G_{12}.

It is suggested that the following areas need more study to develop a more comprehensive model for the MOS: the physics of the drain diode in both the bulk silicon device and the silicon-on-sapphire device; development of different semiconductor materials which have greater mobility and carrier saturation velocity.

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APPENDIX

Solution of the Differential Equation

Expanding (4-16) and using (3-32)

$$\bar{V}(x,t) = V_{ST}(t) - V_{ST}(t) + V_{ST}(t)\sqrt{1 - \frac{x}{L}} \tag{A-1}$$

$$= V_{ST}(t)\sqrt{1 - \frac{x}{L}} \tag{A-2}$$

For small signal inputs a Taylor series expansion will yield

$$\bar{V}(x,t) = V_{ST}\sqrt{1 - \frac{x}{L}} + \frac{1}{2}\epsilon(x,t) \tag{A-3}$$

$$\bar{V}(o,t) = V_{ST} + \frac{1}{2}\epsilon(o,t) \tag{A-4}$$

Carrying out the indicated differentiation in (4-20) yields

$$\frac{1}{2\mu}\frac{\partial\epsilon(x,t)}{\partial t} = \left\{\frac{-V_{ST}}{2L\sqrt{1-\frac{x}{L}}} + \frac{1}{2}\frac{\partial\epsilon(x,t)}{\partial x}\right\}^2 + \left\{V_{ST}\sqrt{1-\frac{x}{L}} + \frac{1}{2}\epsilon(x,t)\right\} \cdot$$

$$\left\{-\frac{V_{ST}}{4L^2}\frac{1}{(1-\frac{x}{L})^{3/2}} + \frac{1}{2}\frac{\partial^2\epsilon(x,t)}{\partial x^2}\right\} \tag{A-5}$$

Keeping only first order terms in $\epsilon(x,t)$

$$\frac{\partial\epsilon}{\partial t} = \mu V_{ST}\left\{(1-\frac{x}{L})^{1/2}\frac{\partial^2\epsilon}{\partial x^2} - \frac{1}{L(1-\frac{x}{L})^{1/2}}\frac{\partial\epsilon}{\partial x} - \frac{1}{4L^2(1-\frac{x}{L})^{3/2}}\epsilon\right\} \tag{A-6}$$

Make the substitution

$$z = 1 - \frac{x}{L} \tag{A-7}$$

$$\frac{\partial \varepsilon}{\partial t} = \frac{\mu V_{ST}}{L^2} \left\{ \sqrt{z}\, \frac{\partial^2 \varepsilon}{\partial z^2} + \frac{1}{\sqrt{z}}\, \frac{\partial \varepsilon}{\partial z} - \frac{1}{4z^{3/2}}\, \varepsilon \right\} \tag{A-8}$$

Define

$$\omega_o = \frac{\mu V_{ST}}{L^2} \tag{A-9}$$

Finally

$$\frac{\partial \varepsilon}{\partial t} = \omega_o \left\{ \sqrt{z}\, \frac{\partial^2 \varepsilon}{\partial z^2} + \frac{1}{\sqrt{z}}\, \frac{\partial \varepsilon}{\partial z} - \frac{1}{4z^{3/2}}\, \varepsilon \right\} \tag{A-10}$$

Taking the LaPlace transform of both sides of (A-10), transposing, and multiplying by $z^{3/2}/\omega_o$

$$z^2 \frac{\partial^2 \varepsilon}{\partial z^2} + z \frac{\partial \varepsilon}{\partial z} - \left(\frac{1}{4} + z^{3/2} \frac{s}{\omega_o}\right) \varepsilon = 0 \tag{A-11}$$

The solution for ε becomes

$$\varepsilon(z,s) = C_1 I_{\frac{2}{3}} \left(\frac{4}{3} \sqrt{\frac{s}{\omega_o}}\, z^{3/4}\right) + C_2 I_{-\frac{2}{3}} \left(\frac{4}{3} \sqrt{\frac{s}{\omega_o}}\, z^{3/4}\right) \tag{A-12}$$

where $I_{\frac{2}{3}}$ is the modified Bessel function of the first kind and of order 2/3.

To apply the boundary conditions, they must first be understood. Obviously $\frac{1}{2}\,\epsilon\,(o,t)$ is the input forcing function of the effective gate. Thus

$$\frac{1}{2}\,\epsilon\,(o,t) = v_{ST}(t) \tag{A-13}$$

where

$$V_{ST}(t) = V_{ST} + v_{ST}(t) \tag{A-14}$$

and

$$V_{ST}(t) = \frac{V_G(t) + D\,V_D(t)}{1 + D} \tag{A-15}$$

The voltage at the end of the source region ℓ_s is constrained to be the effective gate voltage. Therefore, since $\bar{V}\,(x,t)$ represents the voltage across the effective gate capacitor, $\bar{V}\,(L,t) = 0$. Thus

$$\epsilon(L,t) = 0 \tag{A-16}$$

Since $I_{-\frac{2}{3}}(0) \to \infty$, and $\frac{4}{3}\sqrt{\frac{s}{\omega_o}}\; z^{3/4} \to o$ as $x \to L$,

$$C_2 = 0 \tag{A-17}$$

Since $\epsilon\,(o,t) = 2v_{ST}(t)$ and since $x \to o$ means $z \to 1$,

$$C_1 = \frac{2v_{ST}(s)}{I_{\frac{2}{3}}\left(\frac{4}{3}\sqrt{\frac{s}{\omega_o}}\right)} \tag{A-18}$$

Therefore

$$\frac{1}{2}\,\epsilon(z,s) = V_{ST}(s)\,\frac{I_{2/3}\left(\frac{4}{3}\sqrt{\frac{s}{\omega_o}}\,z^{3/4}\right)}{I_{2/3}\left(\frac{4}{3}\sqrt{\frac{s}{\omega_o}}\right)} \tag{A-19}$$

From (4-10), (4-13), (4-16), (4-17), and (A-3)

$$I(x,t) = \frac{-\mu}{L}\,C_{GC}\,(1+D)\left\{V_{ST}\sqrt{1-\frac{x}{L}} + \frac{1}{2}\,\epsilon(x,t)\right\}\frac{\partial}{\partial x}\left\{V_{ST}\sqrt{1-\frac{x}{L}} + \frac{1}{2}\,\epsilon(x,t)\right\} \tag{A-20}$$

$$= \frac{-\mu}{L}\,C_{GC}(1+D)\left\{V_{ST}\sqrt{1-\frac{x}{L}} + \frac{1}{2}\,\epsilon(x,t)\right\}\left\{-\frac{V_{ST}}{2L\sqrt{1-\frac{x}{L}}} + \frac{1}{2}\,\frac{\partial\epsilon(x,t)}{\partial x}\right\} \tag{A-21}$$

Keeping only first order terms in $\epsilon(x,t)$

$$I(x,t) = \frac{-\mu}{L}\,C_{GC}(1+D)\left\{-\frac{V_{ST}^2}{2L} + \frac{1}{2}\,V_{ST}\sqrt{1-\frac{x}{L}}\,\frac{\partial\epsilon(x,t)}{\partial x} - \frac{V_{ST}}{4L\sqrt{1-\frac{x}{L}}}\,\epsilon(x,t)\right\} \tag{A-22}$$

Considering only the time dependent portion

$$i(x,t) = \frac{-\mu}{2L}\,C_{GC}\,(1+D)\,\frac{d}{dx}\left(V_{ST}\sqrt{1-\frac{x}{L}}\,\epsilon(x,t)\right) \tag{A-23}$$

$$i(z,s) = \frac{\mu}{2L^2}\,C_{GC}\,(1+D)\,\frac{d}{dz}\left(V_{ST}\sqrt{z}\,\epsilon(z,s)\right) \tag{A-24}$$

Making use of the Bessel function indentities

$$\frac{d}{dz} I_\nu(z) = \frac{1}{2} \left(I_{\nu+1}(z) + I_{\nu-1}(z)\right) \tag{A-25}$$

$$\frac{2\nu}{z} I_\nu(z) = I_{\nu-1}(z) - I_{\nu+1}(z) \tag{A-26}$$

$$i(z,s) = \frac{\mu}{L^2} C_{GC}(1+D)\, V_{ST} v_{ST}(s) \sqrt{\frac{s}{\omega_o}}\, z^{\frac{1}{4}} \left[\frac{I_{-1/3}(\frac{4}{3}\sqrt{\frac{s}{\omega_o}}\, z^{3/4})}{I_{2/3}(\frac{4}{3}\sqrt{\frac{s}{\omega_o}})}\right] \tag{A-27}$$

Using (3-27)

$$i(z,s) = g_{mo}(1+D)\, v_{ST}(s) \sqrt{\frac{s}{\omega_o}}\, z^{1/4} \left[\frac{I_{-1/3}(\frac{4}{3}\sqrt{\frac{s}{\omega_o}}\, z^{3/4})}{I_{2/3}(\frac{4}{3}\sqrt{\frac{s}{\omega_o}})}\right] \tag{A-28}$$

The portion of the drain current i_{d1} is obtained by taking the limit of $i(z,s)$ as $z \to o$. For small values of the argument

$$\lim_{z \to o} I_\nu(z) = \lim_{z \to o} \frac{\left(\frac{z}{2}\right)^\nu}{(\nu+1)} \tag{A-29}$$

Thus

$$i_{d1}(s) = \lim_{z \to o} \frac{g_{mo}(1+D)\, v_{ST}(s) \sqrt{\frac{s}{\omega_o}}\, z^{\frac{1}{4}}}{I_{2/3}(\frac{4}{3}\sqrt{\frac{s}{\omega_o}})} \quad \frac{(\frac{1}{2}\frac{4}{3}\sqrt{\frac{s}{\omega_o}}\, z^{3/4})^{-1/3}}{2/3} \tag{A-30}$$

$$= \frac{g_{mo}(1+D)\ v_{ST}(s)\ (\frac{s}{\omega_o})^{1/3}}{(\frac{2}{3})^{1/3}\ (\frac{2}{3})\ I_{2/3}\ (\frac{4}{3})\sqrt{\frac{s}{\omega_o}})} \qquad \text{(A-31)}$$

Using the relationships

$$\nu\Gamma(\nu) = \Gamma(\nu+1) \qquad \text{(A-32)}$$

and

$$I_\nu(z) = \sum_{n=o}^{\infty} \frac{(\frac{z}{2})^{2n+\nu}}{n!\,\Gamma(n+\nu+1)} \qquad \text{(A-33)}$$

one obtains

$$i_{d1}(s) = g_{mo}(1+D)\ v_{ST}(s)\ \frac{1}{1 + \frac{4}{15}\frac{s}{\omega_o} + \frac{1}{45}(\frac{s}{\omega_o})^2 + \frac{4}{4455}(\frac{s}{\omega_o})^3 + \ldots} \qquad \text{(A-34)}$$

The nth term is given by

$$(n)_{term} = \frac{\frac{4}{3}\frac{s}{\omega_o}}{n(3n+2)}\ (n-1)_{term} \qquad \text{(A-35)}$$

The source current can be obtained by taking the limit of i(z,s) as $z \to 1$.

$$i_s(s) = g_{mo}(1+D)\ v_{ST}(s)\sqrt{\frac{s}{\omega_o}}\ \frac{I_{-1/3}(\frac{4}{3}\sqrt{\frac{s}{\omega_o}})}{I_{2/3}(\frac{4}{3}\sqrt{\frac{s}{\omega_o}})} \qquad \text{(A-36)}$$

Using (A-32) and (A-33) the result is

$$i_s(s) = g_{mo}(1+D)\, v_{ST}(s)\, \frac{1 + \frac{2}{3}\frac{s}{\omega_o} + \frac{4}{45}\left(\frac{s}{\omega_o}\right)^2 + \frac{2}{405}\left(\frac{s}{\omega_o}\right)^3 + \ldots}{1 + \frac{4}{15}\frac{s}{\omega_o} + \frac{1}{45}\left(\frac{s}{\omega_o}\right)^2 + \frac{4}{4455}\left(\frac{s}{\omega_o}\right)^3 + \ldots} \qquad \text{(A-37)}$$

The nth term in the numerator is given by

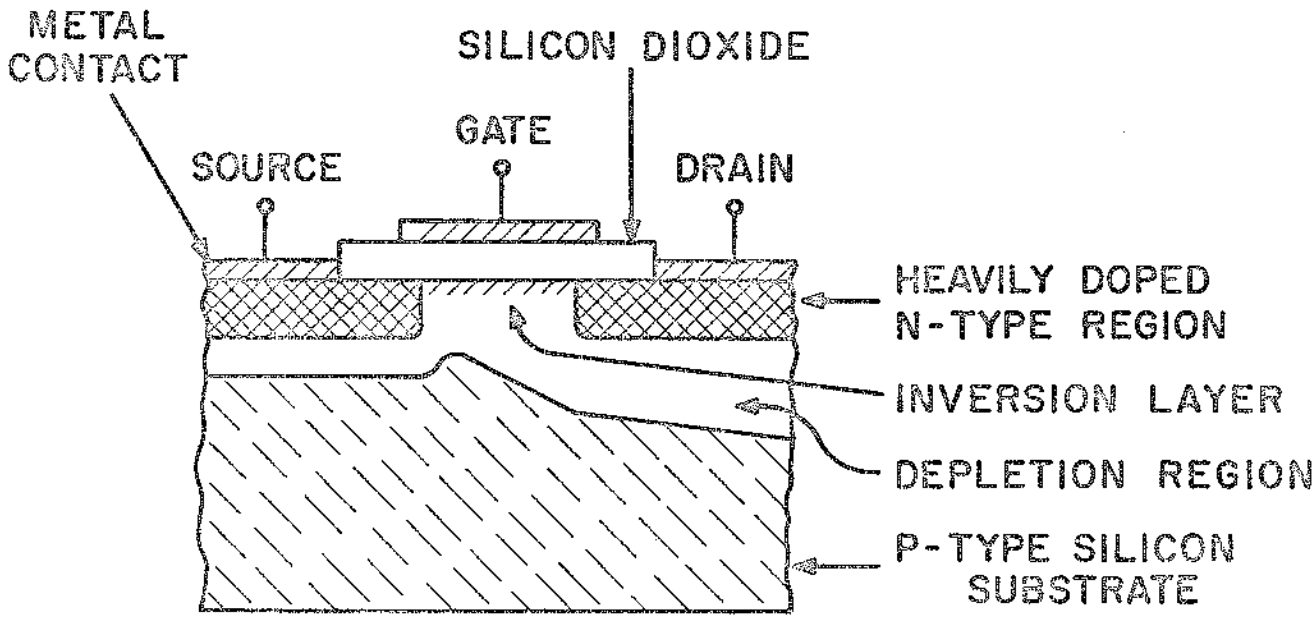
$$(n)_{term} = \frac{4\,\frac{s}{\omega_o}}{3n(3n-1)}\ (n-1)_{term} \qquad \text{(A-38)}$$

From FIG. 4-2

$$i_{ST}(s) = i_s(s) - i_{dl}(s) \qquad \text{(A-39)}$$

then

$$i_{ST}(s) = g_{mo}(1+D)\, v_{ST}(s)\, \frac{\frac{2}{3}\frac{s}{\omega_o} + \frac{4}{45}\left(\frac{s}{\omega_o}\right)^2 + \frac{2}{405}\left(\frac{s}{\omega_o}\right)^3 + \ldots}{1 + \frac{4}{15}\frac{s}{\omega_o} + \frac{1}{45}\left(\frac{s}{\omega_o}\right)^2 + \frac{4}{4455}\left(\frac{s}{\omega_o}\right)^3 + \ldots} \qquad \text{(A-40)}$$



NORMAL OPERATION: SOURCE AND SUBSTRATE GROUNDED, GATE POSITIVE, DRAIN MORE POSITIVE.

INPUT: GATE VOLTAGE. OUTPUT: DRAIN CURRENT.

FIG. 1-1 MOS BULK SILICON STRUCTURE

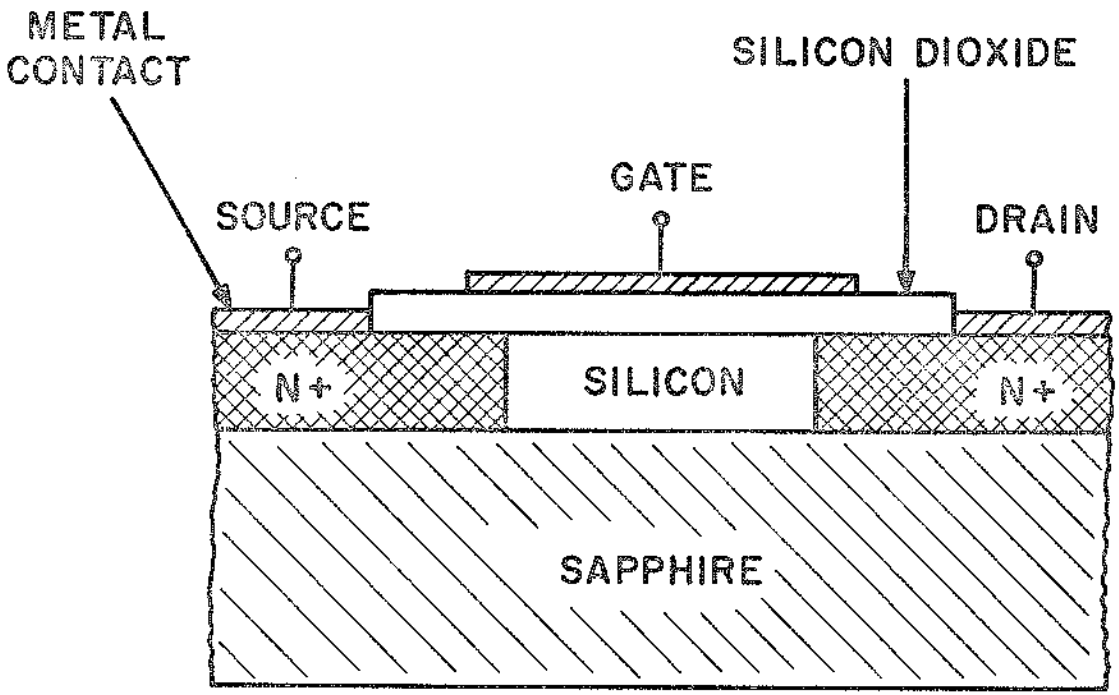


FIG. I-2 MOS SILICON-ON-SAPPHIRE STRUCTURE

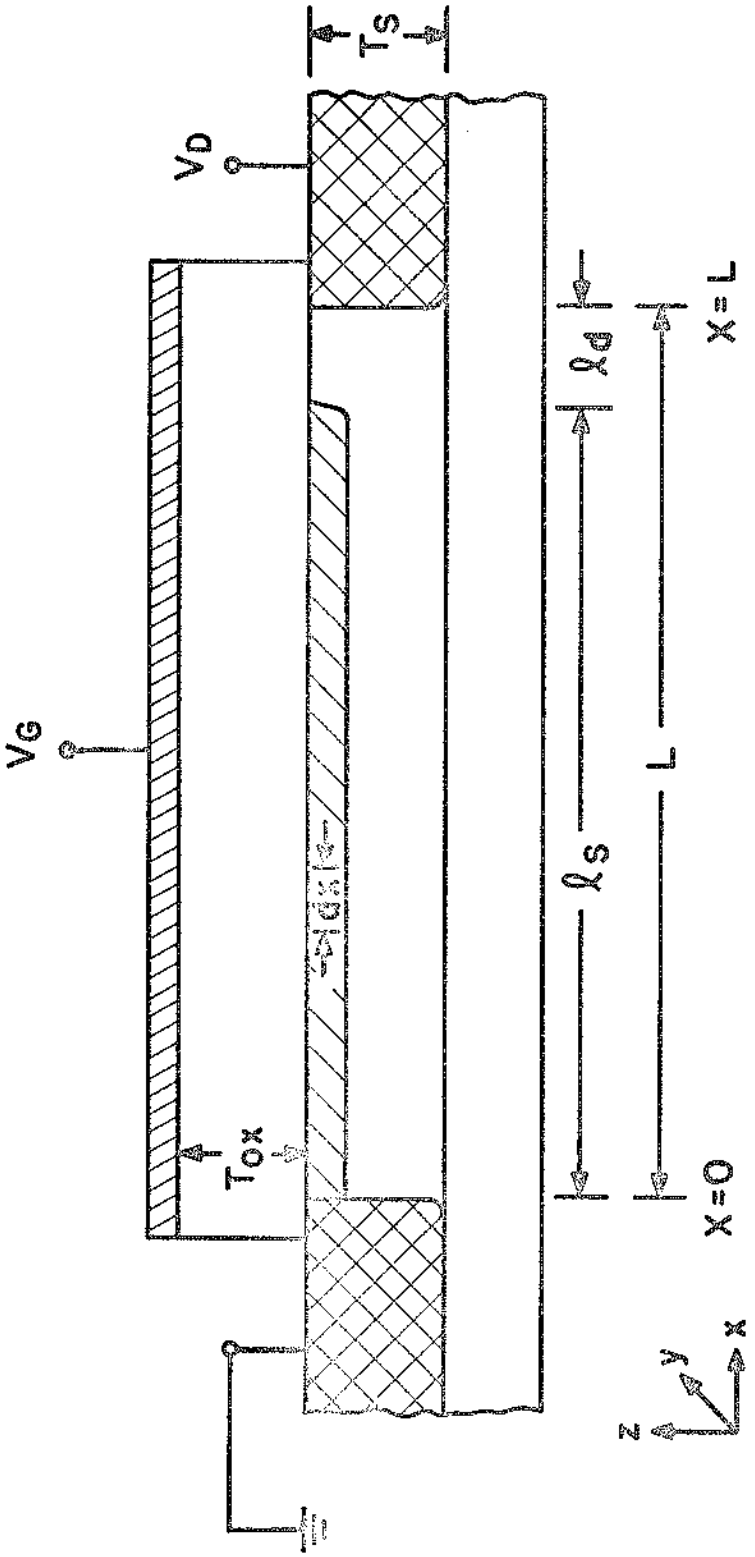


FIG. 2-1 DEFINITION OF DIMENSIONS IN MOS EQUATIONS

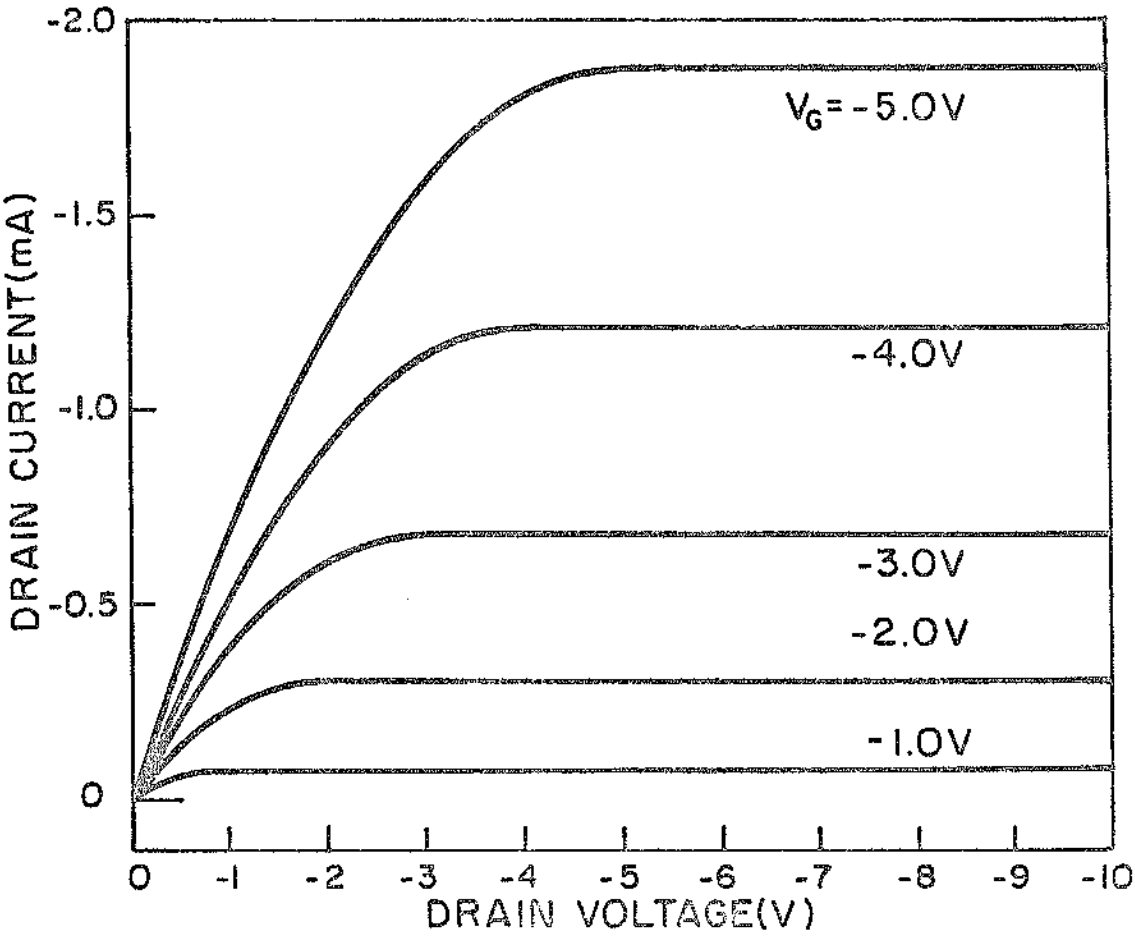


FIG. 2-2 BASIC THEORETICAL I-V CURVES FOR MOS

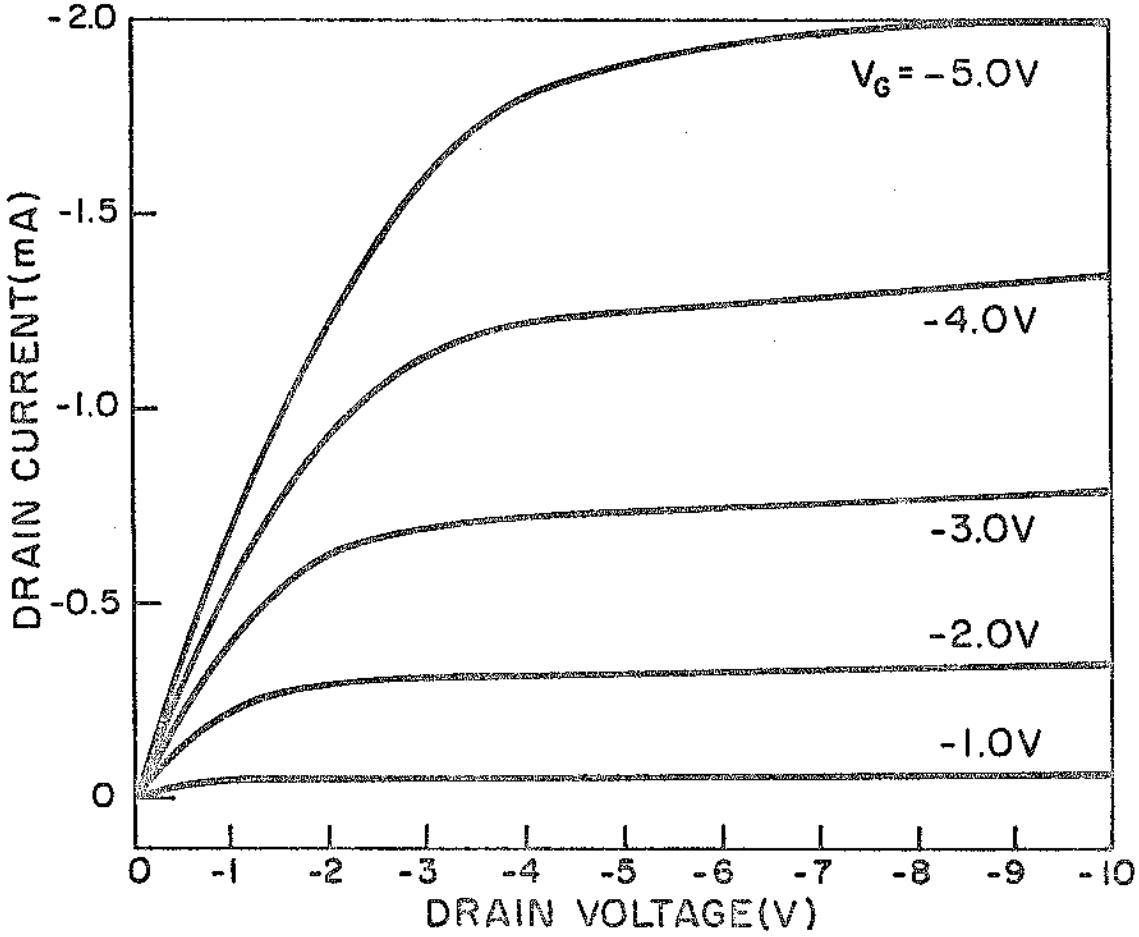


FIG. 2-3 I-V CURVES FOR DEVICE 6-7-8

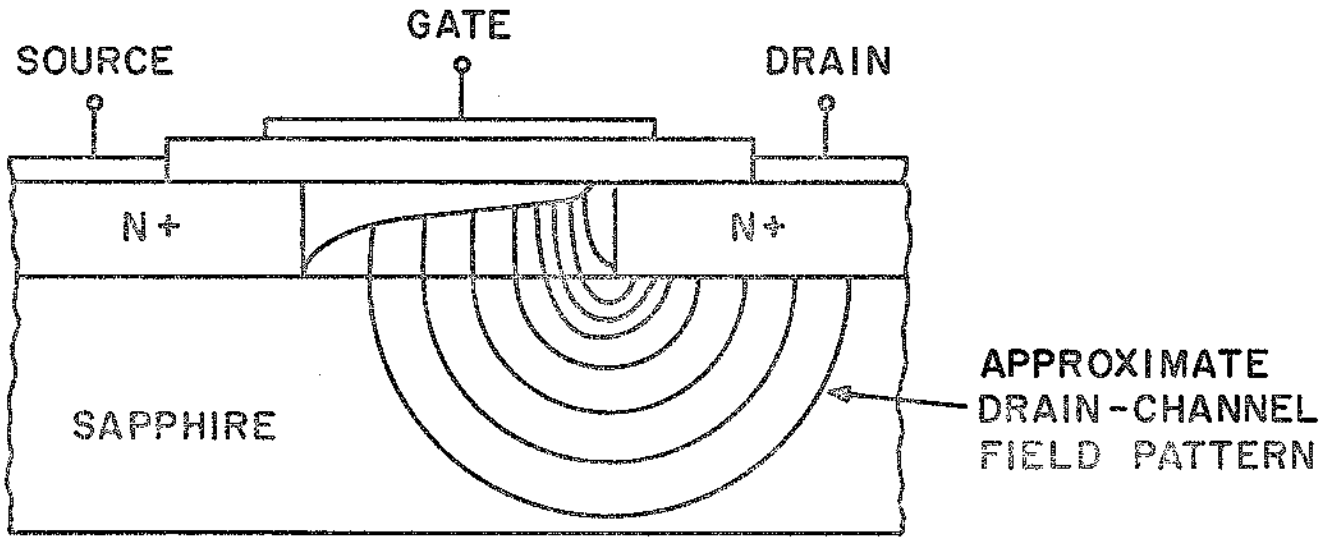


FIG. 3-1 MODEL FOR CALCULATING DC DRAIN CONDUCTANCE (FROM HEIMAN & HOFSTEIN[10])

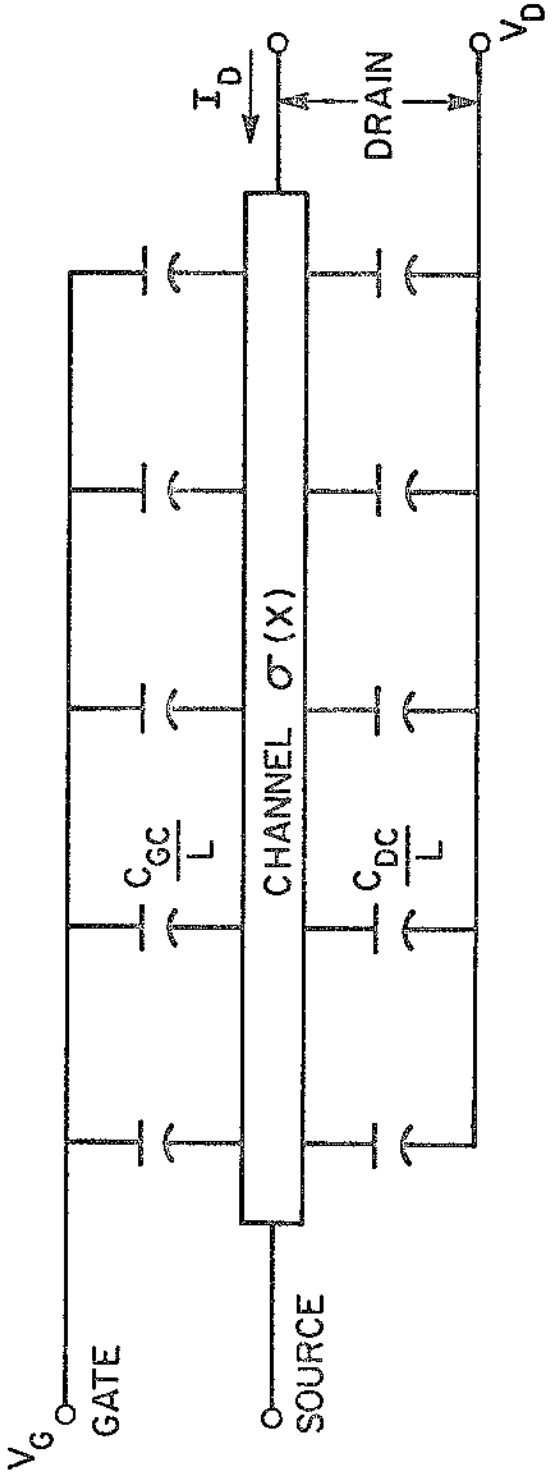


FIG. 3–2 DC MODEL OF THE MOS

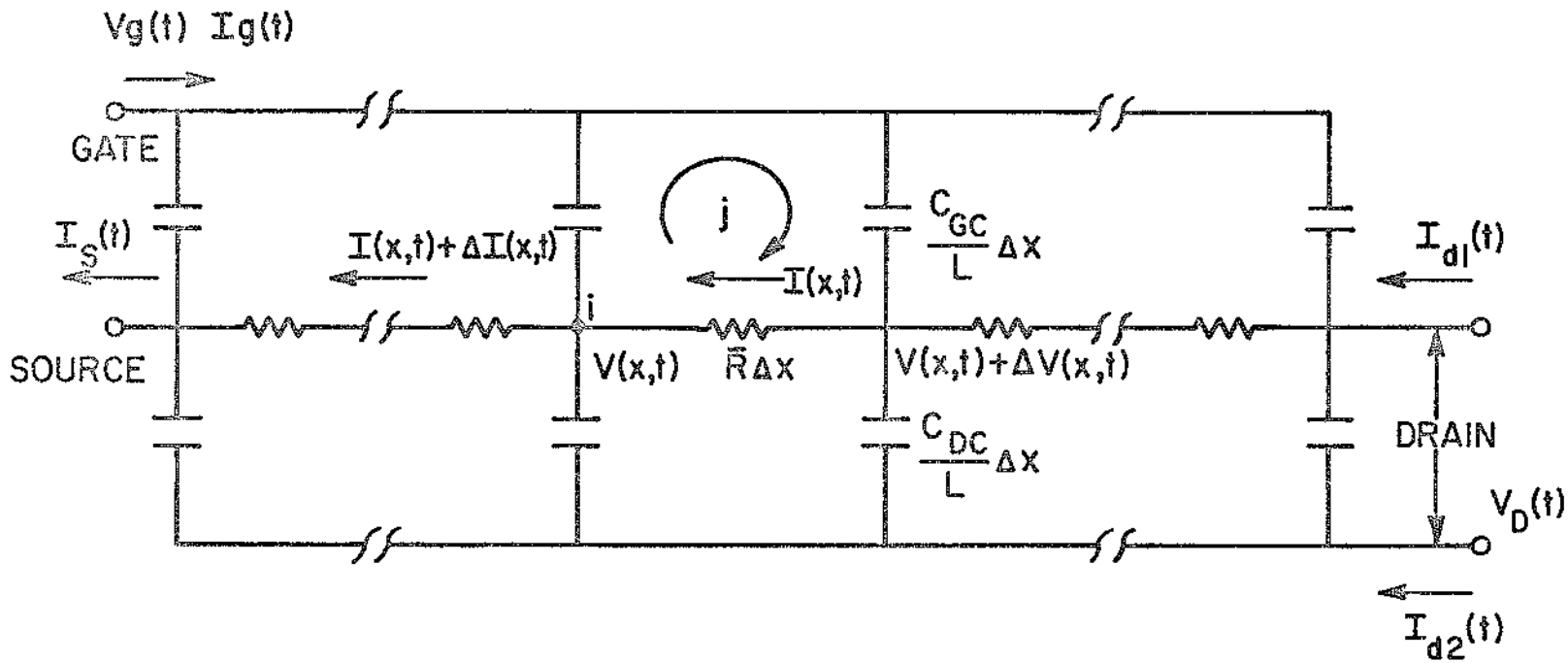


FIG. 4—1 HIGH-FREQUENCY MODEL OF THE MOS

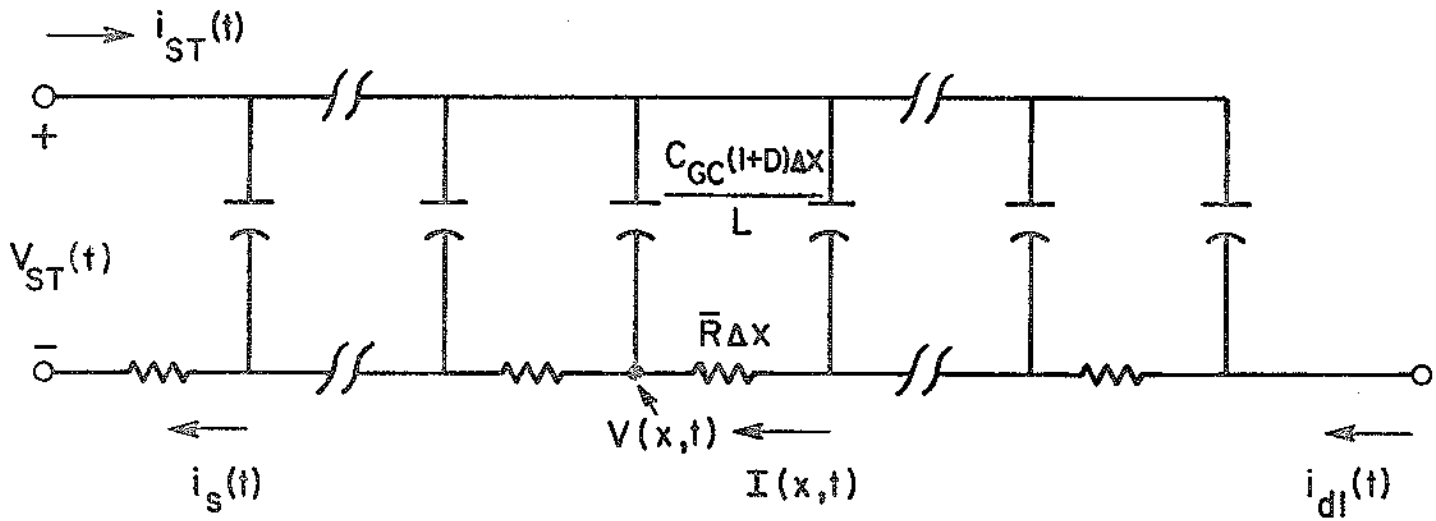


FIG. 4-2 CIRCUIT EQUIVALENT TO FIG.4-1.

DRAIN-CHANNEL INTERACTION IS CONTAINED IN $V_{ST}(t)$

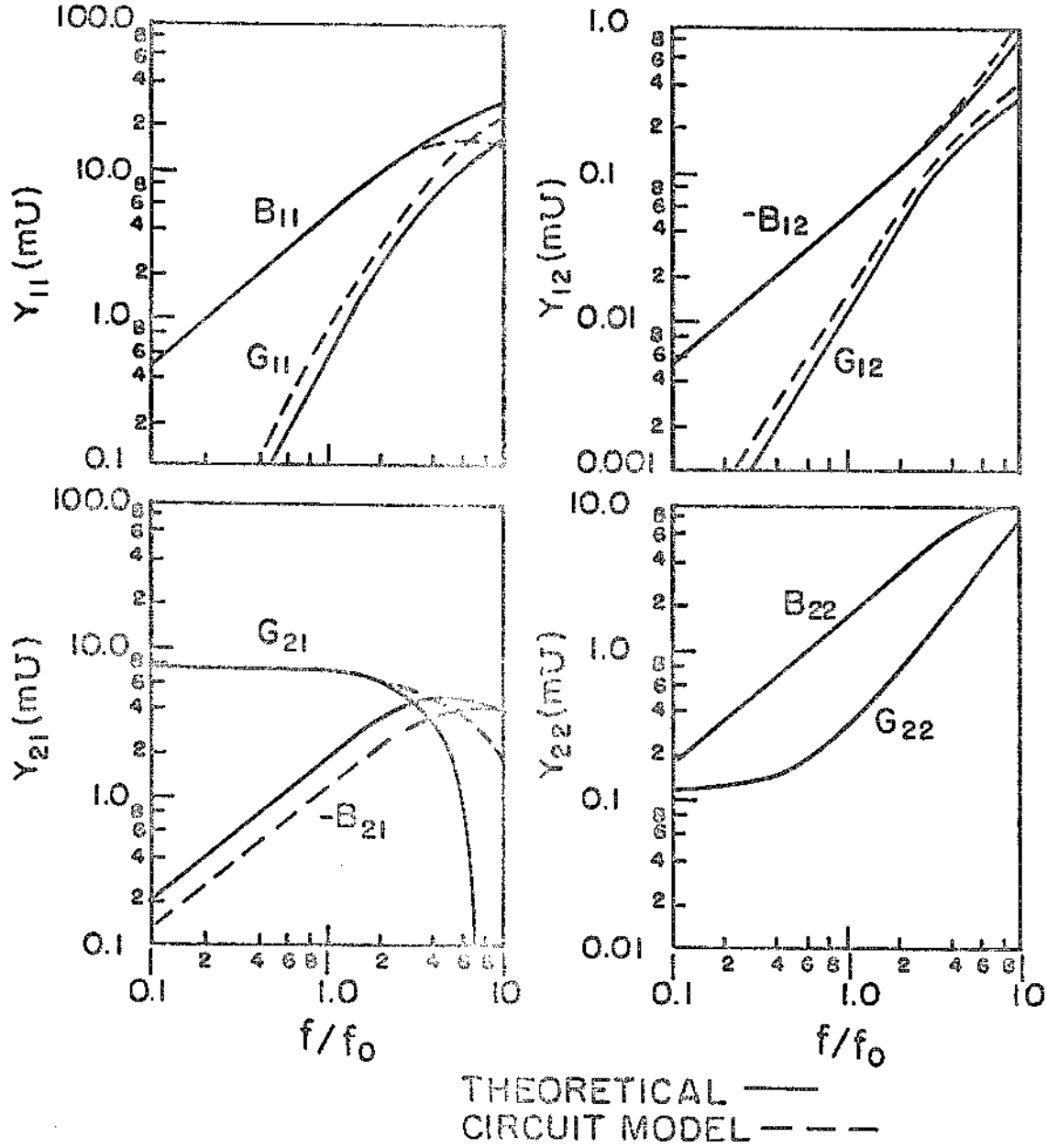


FIG. 6-1 COMPARISON OF THEORETICAL Y-PARAMETERS AND CIRCUIT MODEL Y-PARAMETERS

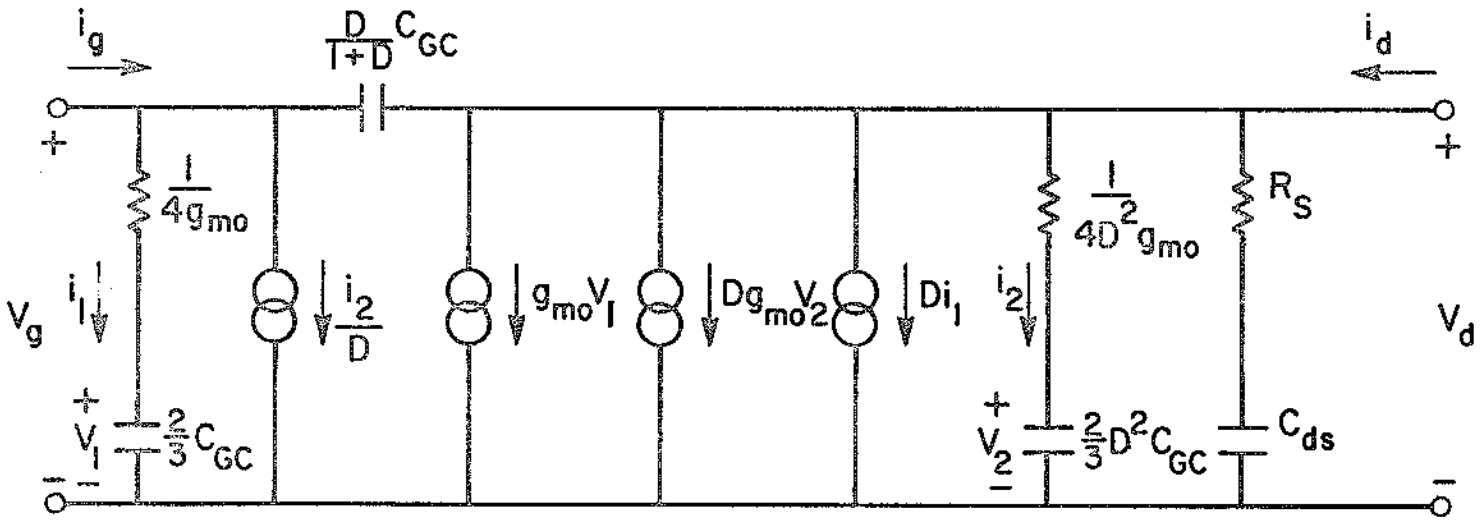


FIG. 6–2 APPROXIMATE EQUIVALENT CIRCUIT OF THE MOS

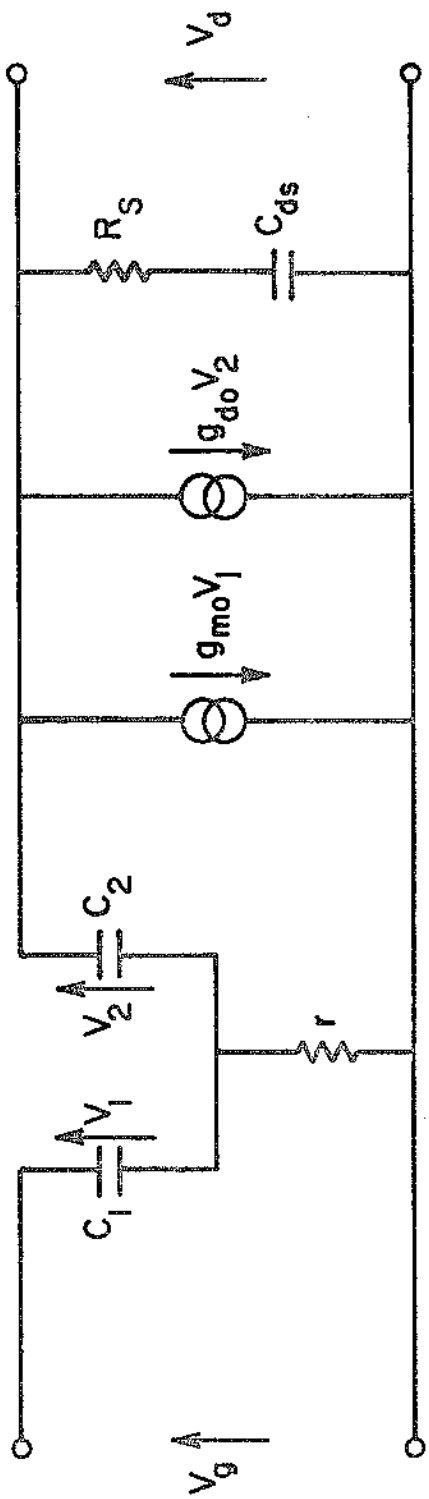
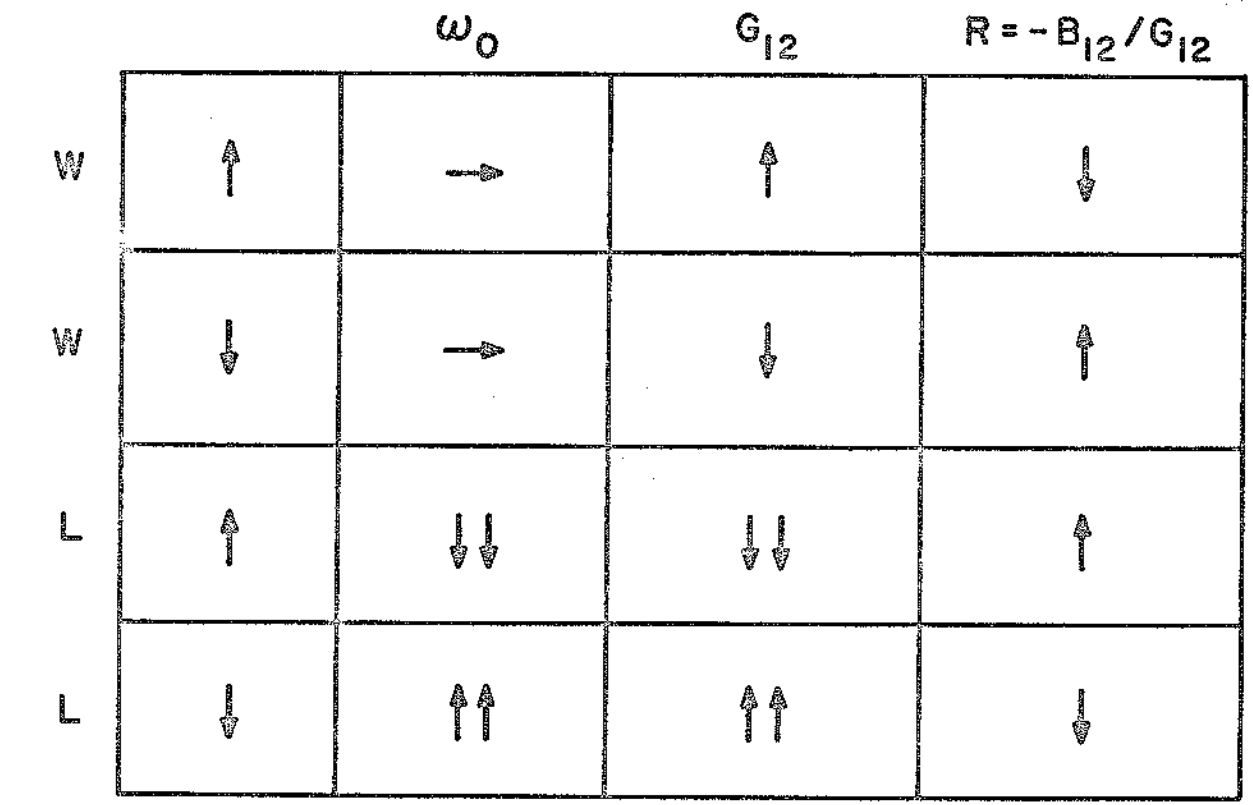


FIG. 6-3 MODEL OF THE MOS PROPOSED BY DAWSON [13]



SYMBOL DEFINITIONS: → CONSTANT ↑ LINEAR INCREASE

↓ LINEAR DECREASE ↑↑ SQUARE INCREASE

↓↓ SQUARE DECREASE

FIG. 7-1 TABLE SHOWING DEPENDENCE OF ω_0, G_{12}, AND R ON W AND L.

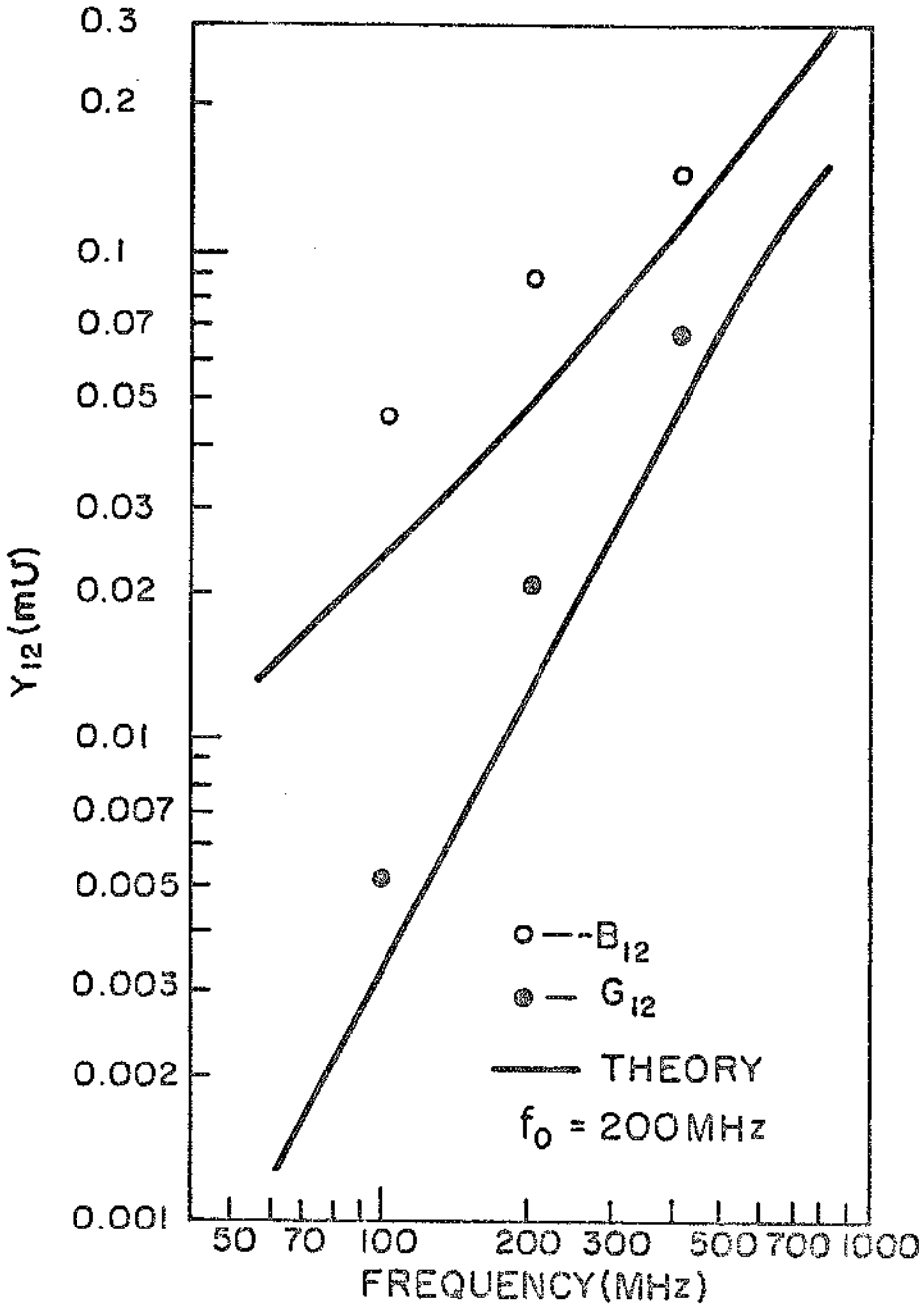


FIG. 7-2 EXPERIMENTAL AND THEORETICAL Y_{12} vs. FREQUENCY FOR 3N142

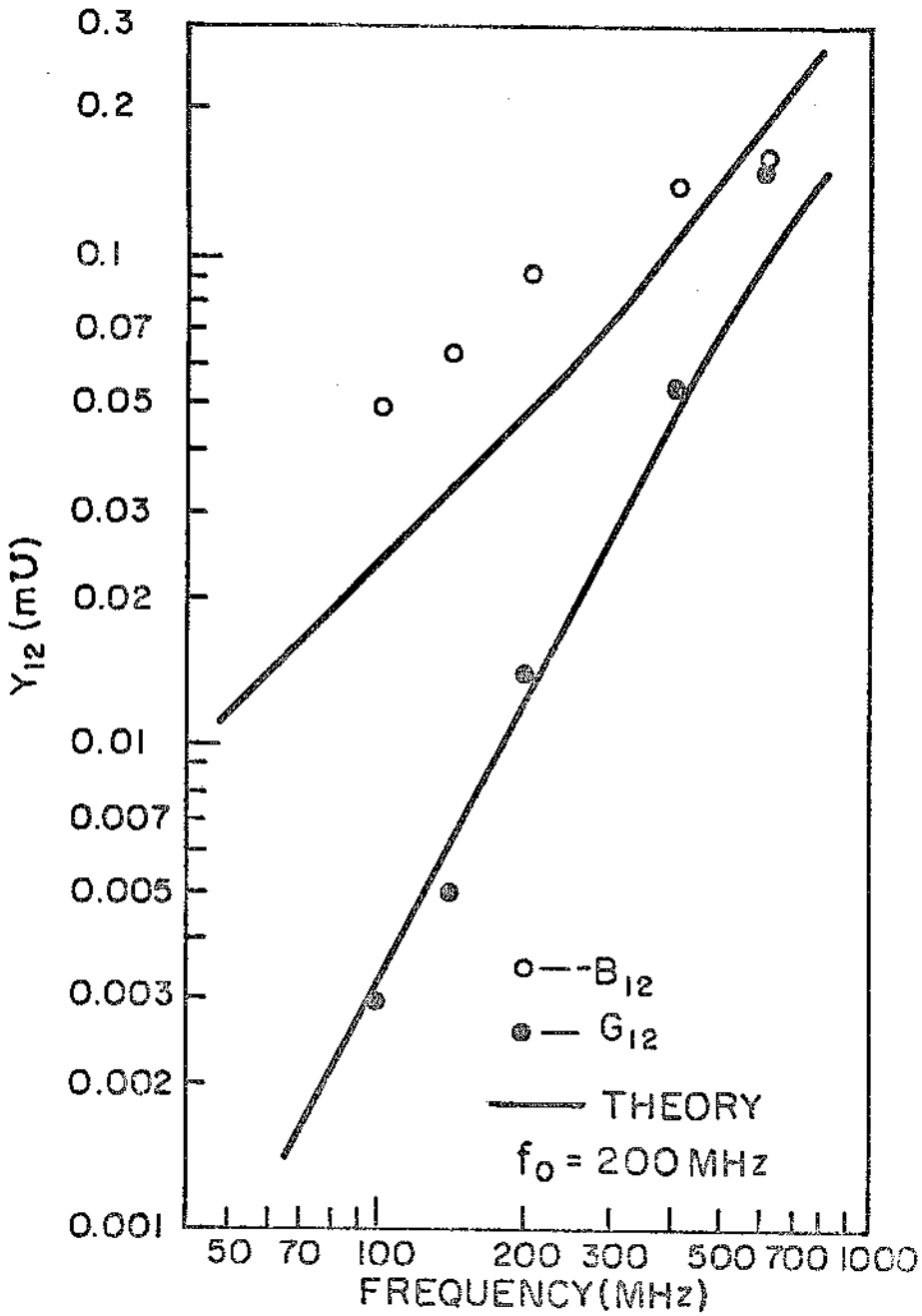


FIG. 7-3 EXPERIMENTAL AND THEORETICAL Y12 vs. FREQUENCY FOR 40468

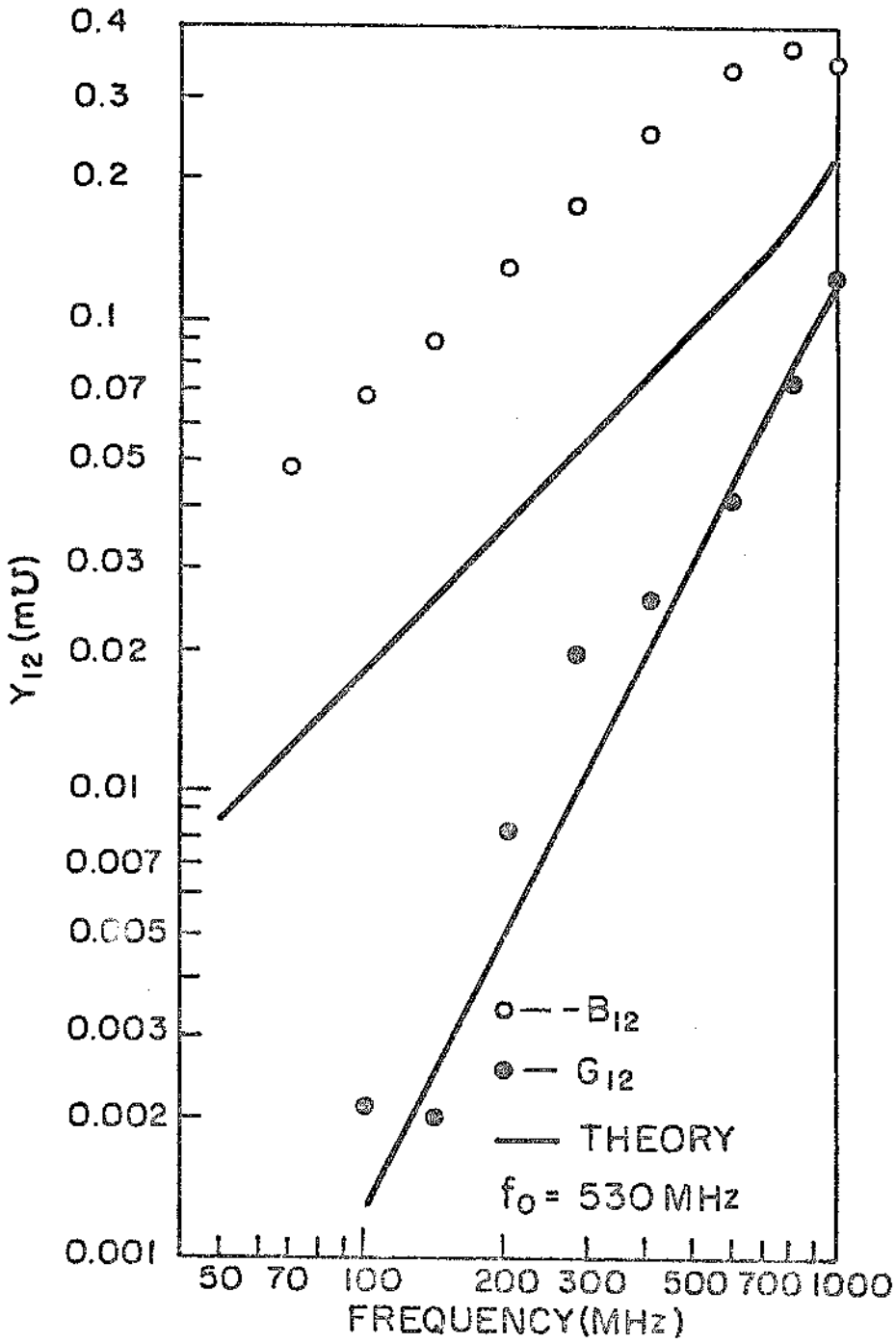


FIG. 7-4 EXPERIMENTAL AND THEORETICAL Y_{12} VS. FREQUENCY FOR TRIODE LOT 929

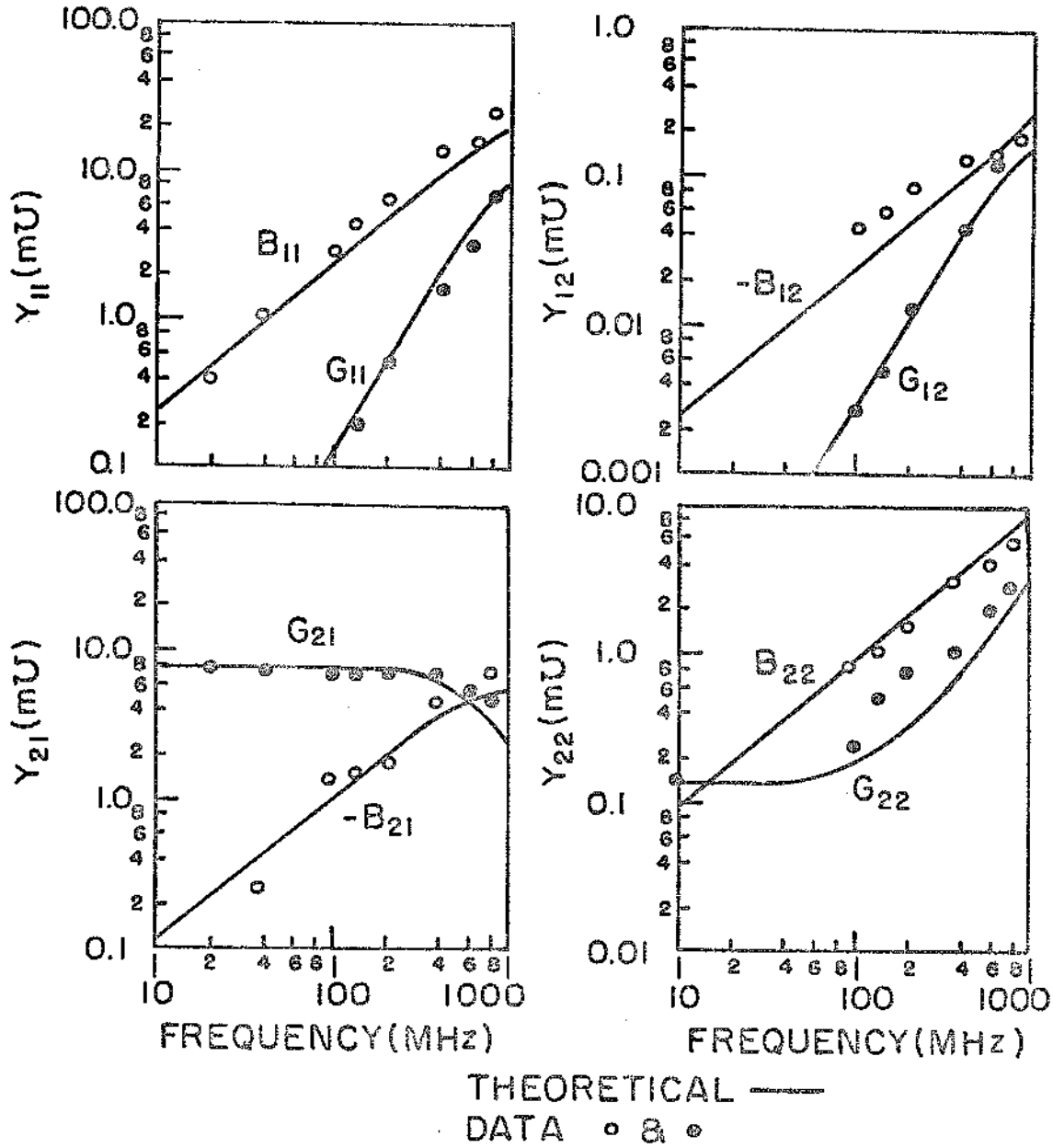


FIG. 7-5 COMPARISON OF THEORETICAL Y-PARAMETERS AND MEASURED Y-PARAMETERS FOR 40468

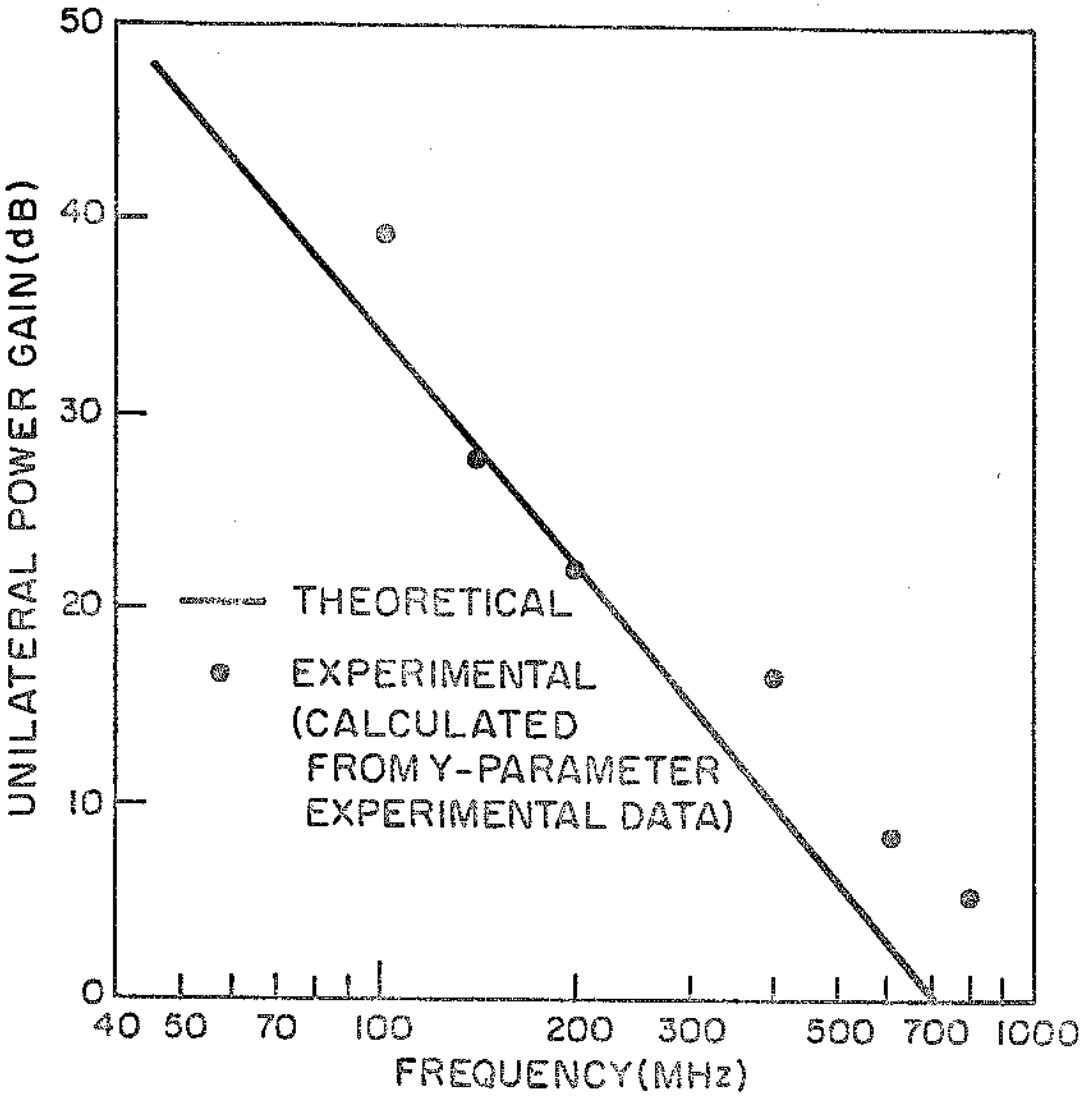


FIG. 7-6 UNILATERAL POWER GAIN vs. FREQUENCY FOR THE 40468

V_{ii} INCIDENT VOLTAGE - INPUT

V_{ri} REFLECTED VOLTAGE - INPUT

V_{io} INCIDENT VOLTAGE - OUTPUT

V_{ro} REFLECTED VOLTAGE - OUTPUT

$$S_{11} = \left.\frac{V_{ri}}{V_{ii}}\right|_{V_2=0} \qquad S_{12} = \left.\frac{V_{ri}}{V_{io}}\right|_{V_1=0}$$

$$S_{21} = \left.\frac{V_{ro}}{V_{ii}}\right|_{V_2=0} \qquad S_{22} = \left.\frac{V_{ro}}{V_{io}}\right|_{V_1=0}$$

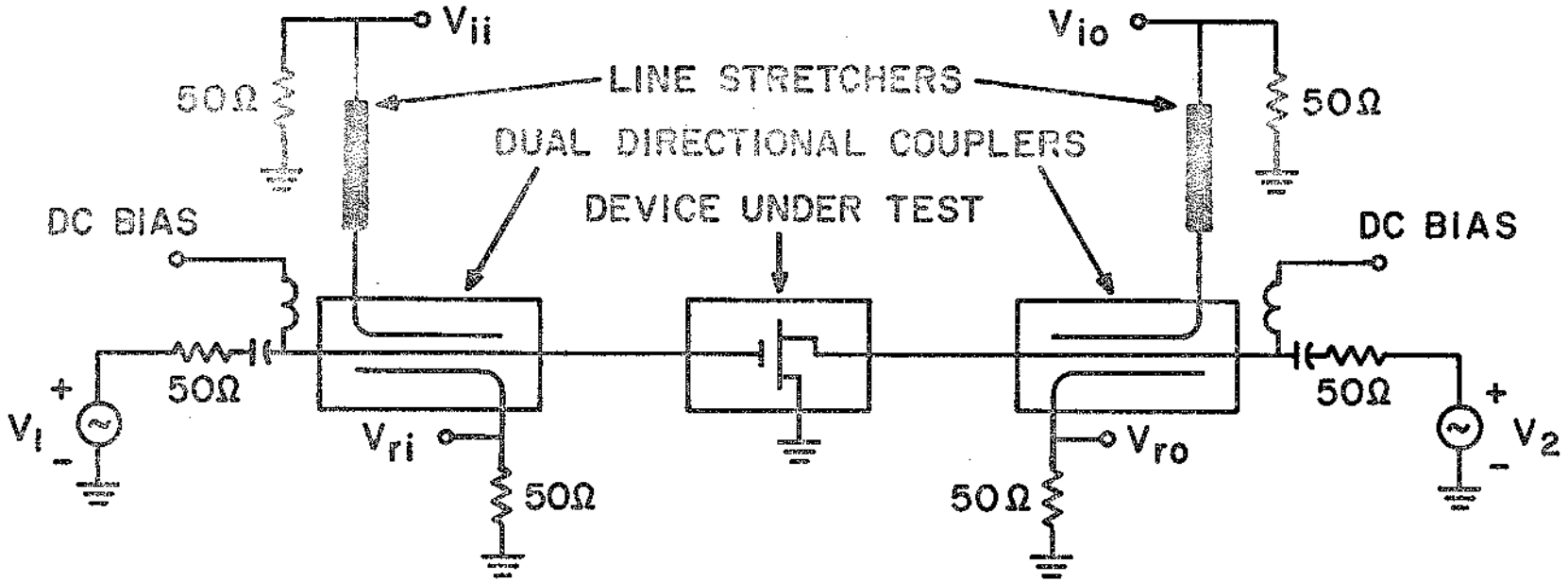


FIG. 7-7 S-PARAMETER SET-UP AND DEFINITION

Robert S. Hopkins Jr.

1942	Born October 26 in Bevinsville, Kentucky
1960	Graduated from Holton High School, Holton, Indiana
1963-64	Junior Engineer, Arvin Electronics Laboratory, West Lafayette, Indiana
1964	B.S.E.E., Purdue University
1964	Member of the Technical Staff, RCA Laboratories, Princeton, New Jersey
1964-67	RCA Laboratories Graduate Study Program
1966-67	RCA Laboratories Doctoral Study Award
1967	M.S., Rutgers University
1968	M.Phil, Rutgers University
1970	Ph.D., Rutgers University